A 600MHz to 3.4GHz Flexible Spectrum-Sensing Receiver with Spectrum-Adaptive Reconfigurable DT Filtering

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***Abstract* — A flexible spectrum-sensing receiver in 65nm CMOS consists of a wideband front-end, spectrum-adaptive (SA) filtering, switched-capacitor amplifiers, and a filtering SAR ADC. The SA filter uses a DT spectrum-analyzer and a reconfigurable DT notch filter to detect and suppress large interferers over a 55MHz range. In IEEE 802.15.4 tests, the receiver exceeds sensitivity and interferer rejection requirements. With SA filtering enabled, it achieves ≥+55dB rejection of +25 to +65MHz FM interferers.**

***Index Terms* — Discrete-time filter, SAR ADC, software-defined radio, spectrum-sensing, wireless receiver.**

I. Introduction

The wireless communication spectrum has become increasingly congested in terms of both the diversity of wireless standards and the number of users sharing limited spectrum. Recent research has focused on the first part of the congestion issue, leading to many successful software-defined radio (SDR) techniques, such as a highly linear front-end with tunable analog filters [1], frequency-translated RF and IF bandpass filters [2], and a configurable filtering SAR ("SARfilter") ADC [3]. Although these techniques achieve their performance goals, they inefficiently utilize hardware and power by always assuming the worst-case operating environment.

We propose a spectrum-sensing (SS) method specialized for detecting and adaptively filtering large interferers. Existing spectrum-sensing techniques implement high-sensitivity detection of licensed users for cognitive radios [4] or are digital [5] and require a high-speed, high-resolution ADC and anti-aliasing filtering to digitize the entire band of interest. Both approaches are too complex and high-power to perform spectrum-analysis for adaptive interferer suppression. Therefore, we introduce a low-power analog discrete-time (DT) spectrum-sensing technique, based on the scaling-friendly and robust charge-domain filtering concept together with active digital control of the DT sampling clocks.

Spectrum-sensing enables the receiver to adapt to changing conditions while using fewer circuit resources and less power. Without spectrum-sensing (SS), we would have to overdesign the filters to attenuate all potential interferers, even if we can reasonably expect only a limited number of simultaneous interferers. Instead, we create a spectrum-adaptive (SA) filter by combining analog DT SS along with real-time digital control of the rejection mode of a reconfigurable filter. We demonstrate SA filtering in a complete flexible receiver (Fig. 1), consisting of a wideband front-end, transimpedance amplifier (TIA), a four-mode SS-guided analog DT notch filter, switched-capacitor (SC) amplifiers, and a 7-bit SARfilter ADC that performs additional filtering and digitization. The prototype achieves SA filtering of interferers that are offset 15MHz to 70MHz from a wanted signal. Achieving attenuation over this frequency range

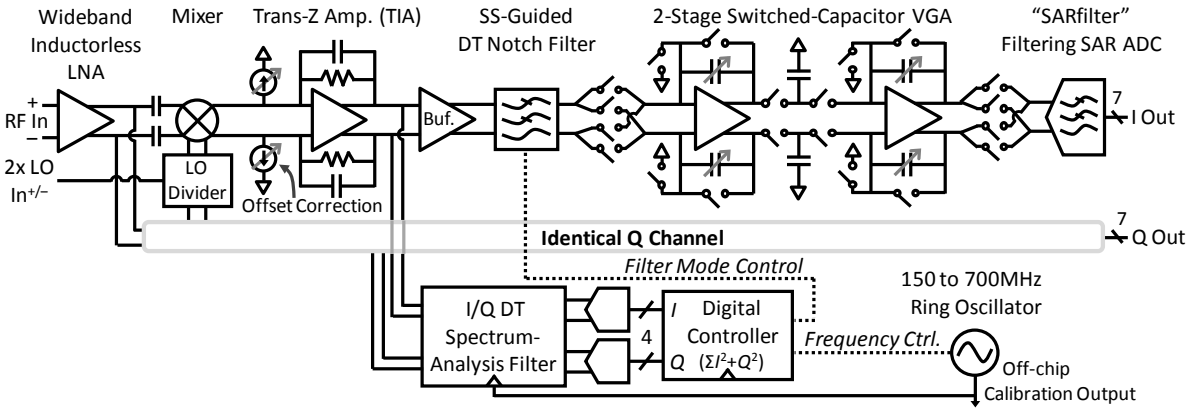

Fig. 1. Architecture of the prototype spectrum-sensing receiver. The spectrum-sensing path (bottom) scans to detect large interferers and automatically selects the optimal rejection mode of the reconfigurable DT notch filter.

with a conventional FIR filter would require two to four times more filter taps and consume proportionally more power and area.

II. Spectrum Sensing

Our proposed spectrum-sensing technique uses identical, frequency-programmable *analog* DT bandpass spectrum-analysis filters in the I and Q channels and simple digital signal processing (DSP). The spectrum-analysis filters isolate and subsample the interferer power contained within select frequency bands. Spectrum-analysis in the analog DT domain eliminates the anti-aliasing filters and high-speed, high-resolution ADCs that digital spectrum-analysis would otherwise require. Analog charge-domain DT filters [6], which consist of switches and capacitors (i.e. no op-amps), are also advantageous because switches function well in nanometer CMOS and the filter response is well-defined by capacitor matching and clocking and independent of process variation.

We introduce a DT spectrum-analysis filter with an easily and accurately tunable center frequency of the power detection passband. This passband is always located at one-tenth of a clocking frequency, f_s. An on-chip ring-oscillator (Fig. 1) generates f_s, so a digital controller can tune the passband frequency by adjusting the oscillator's load capacitance to values calibrated for process variation. The passband frequency ranges from 15 to 70MHz in 5MHz steps and typical calibration inaccuracy or open-loop drift of f_s of less than 3MHz results in a 10x smaller frequency offset of the passband. Importantly, the controller also adjusts filter parameters at each f_s to preserve the passband's gain and bandwidth.

The digital controller (Fig. 1) interprets the output of the spectrum-analysis filter to perform SA filtering. The controller calculates and accumulates I^2+Q^2 for up to 64 filter output samples to measure the interferer's power within each passband. It makes this measurement for every frequency bin, and then directs the notch filter to reject the bin with the greatest measured power.

Fig. 2 shows one of the identical I and Q branches of the four-stage DT spectrum-analysis filter and an example frequency response for each stage when f_s is 250MHz. The four filtering stages together generate notches and poles that create a distinct power detection passband at $f_s/10$. Table I summarizes the sampling rates and frequency responses of the four stages. In the 1st stage, integration sampling creates a lowpass sinc-like response and three time-interleaved channels permit simultaneous sampling, output, and reset. In the 2nd and 3rd stages, pole-zero cancellation between a 5-tap FIR filter and an IIR filter results in a wanted pole at $f_s/10$ and additional poles at $0.9f_s$, $1.1f_s$, $1.9f_s$.... A one-pole roll-off in the TIA and the notches created by the 1st stage attenuate these

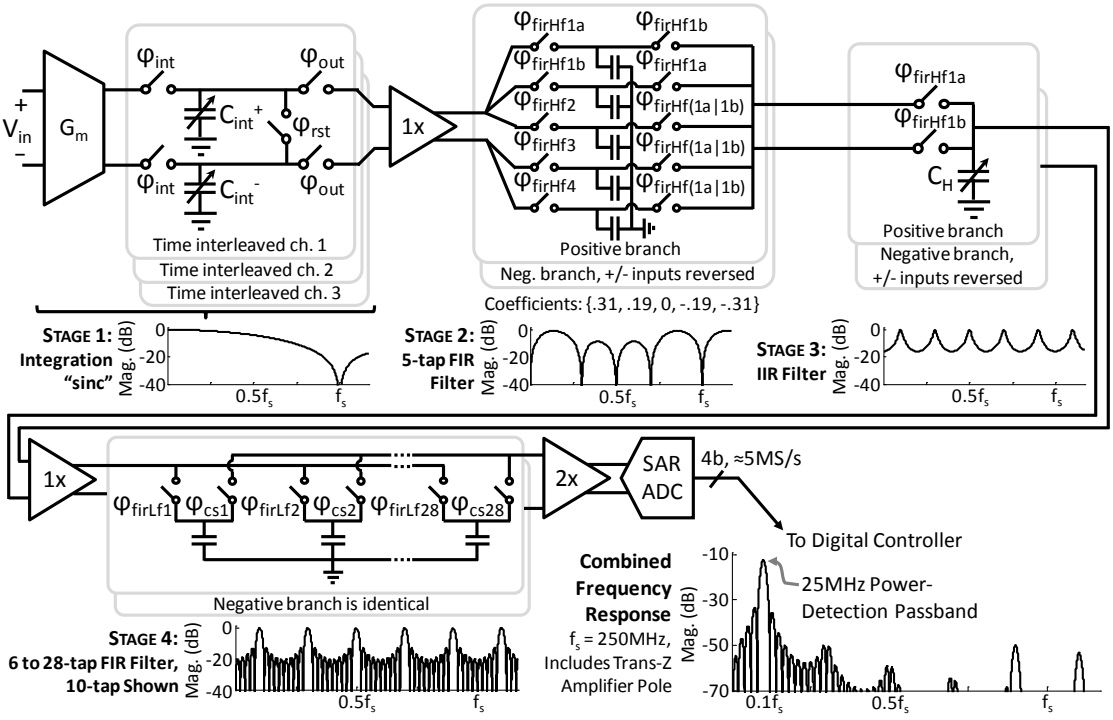

Fig. 2. One of the identical I and Q branches of the four-stage DT bandpass spectrum-analysis filter, including the filter response of each stage. The combined response shows that the spectrum-analysis filter and the TIA pole create a distinct power detection passband.

TABLE I
STAGES OF THE SPECTRUM-ANALYSIS FILTER

Stage	Rate In	Rate Out	Frequency Response
1	f_s	f_s	sinc-like, notches at $n \cdot f_s$, n=1,2,3…
2	f_s	$f_s/5$	notches at DC, $0.3f_s$, $0.5f_s$, $0.7f_s$, f_s…
3	$f_s/5$	$f_s/5$	poles at $0.1f_s$, $0.3f_s$, $0.5f_s$….
4	$f_s/5$	$f_s/140$ to $f_s/30$, always	notches at 0, 5, 10MHz... except at $0.1f_s$, $0.3f_s$, $0.5f_s$...
Combined	f_s	≈5MS/s	power detection passband at $f_s/10$

additional poles. Fig. 2 shows that the combined frequency response of this four-stage DT filter and the TIA roll-off strongly rejects all frequencies outside of the passband.

We enable the use of power-efficient 4-bit SAR A/D conversion and low-frequency DSP by having a fixed output rate. In the 4th stage, a variable rate 6- to 28-tap FIR decimation filter reduces the filter's output rate to ≈5MS/s for all f_s. Furthermore, as the passband's center frequency increases, the controller decreases $C_{int}^{+/-}$ to keep the gain constant and increases C_H and the decimation factor of stage 4 to keep the bandwidth constant.

III. SPECTRUM-ADAPTIVE RECEIVER

We demonstrate the new spectrum-adaptive filtering technique in a flexible direct conversion receiver (Fig. 1) that combines the SA filter with a wideband front-end, TIA, SC amplifiers, and a 7-bit SARfilter ADC with embedded DT filtering. A wideband LNA drives current through the mixer and into a TIA. Current DACs source counteracting currents through the TIA's feedback resistors to remove DC offsets. The TIA drives the G_m stage (Fig. 2) in the SS path (Fig. 1, lower branch) and the reconfigurable DT FIR notch filter through a buffer in the main signal path (Fig. 1, upper branch).

Fig. 3 shows a schematic of a differential half-bank of the 6-tap SS-guided FIR notch filter, which consists of 22 unit capacitors and switches. The input signal, V_{in}, is

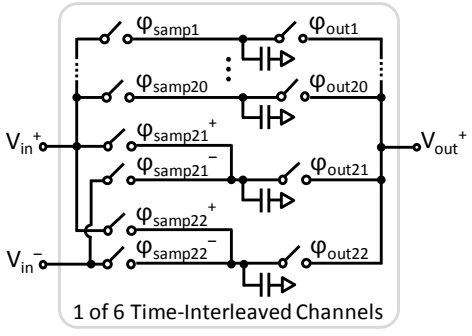

Fig. 3. Schematic of the SS-guided reconfigurable DT FIR notch filter consisting of six time-interleaved channels, each with 22 unit capacitors (per differential half circuit). Two capacitors connect to both $V_{in}^{+/-}$ to implement negative filter coefficients.

sampled onto different combinations of the capacitors (Table II) at 100MS/s, in order to implement four attenuation modes, each with notches that attenuate a different band of the SS frequency range. The number of actively used capacitors changes with the filtering mode. Since a 6-tap analog FIR filter decimates the sampling rate by 6x, we also time-interleave six identical filter channels to achieve equal input and output rates.

After the SS-guided filter, two stages of SC amplifiers (Fig. 1) amplify the output of the notch filter by 21dB to 35dB. Digitally-tunable capacitances in the 1st stage scale proportionally to the number of active unit capacitors in each notch filter mode to preserve gain. Digitally-tunable capacitances in 2nd stage implement variable gain. Chopping switches at the input and output of the 1st and 2nd stages, respectively, reduce 1/f noise.

A SARfilter ADC [3], which embeds a reconfigurable DT FIR/IIR filter within a SAR ADC, further attenuates interferers before performing 7-bit digitization. FIR filtering in the ADC is created by interleaving SAR conversion with multi-cycle sampling of the input onto the capacitive DAC of the ADC. IIR filtering is created by intermediate charge-sharing of these samples with a history capacitor. The spectrum-adaptive filter attenuates large interferers offset 15 to 70MHz from the wanted signal, the TIA pole attenuates higher frequency interferers, and the lowpass SARfilter ADC attenuates outside of the channel bandwidth.

IV. MEASURED PERFORMANCE

The prototype receiver is implemented in 65nm CMOS. Fig. 4 shows a die photo. The prototype achieves 55.8dB gain and supports carrier frequencies from 600MHz to 3.4GHz. Fig. 5 plots the combined frequency response of the receiver, which includes the attenuation of the TIA pole, the SS-guided filter disabled and in mode 3 (Table II), and the SARfilter ADC. The SS-guided filter in mode 3 contributes an average of 26dB additional attenuation

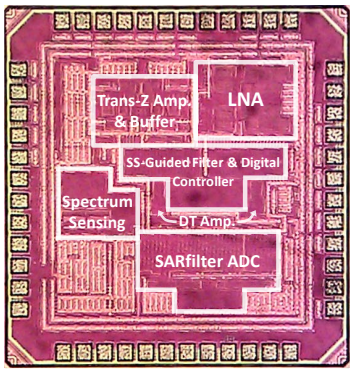

Fig. 4. Die photo of the 65nm CMOS prototype receiver.

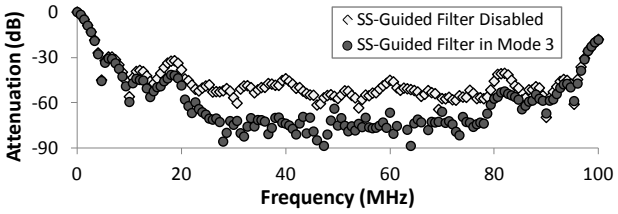

Fig. 5. Measured combined frequency response of the receiver when the SS-guided filter is disabled or in mode 3. Compared to when filtering is disabled, mode 3 provides an average of 26dB more attenuation of the target 28-42MHz and 58-70MHz bands.

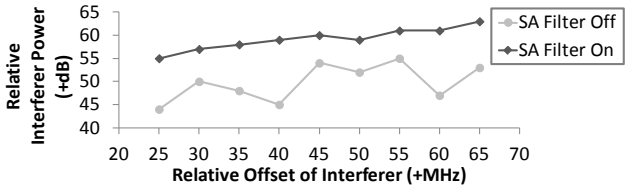

Fig. 6. Measured relative power vs. frequency offset of an FM interferer (1MHz deviation, 50kHz rate) at which the receiver achieves 1% PER when receiving RF modulated IEEE 802.15.4 2450MHz band packets with -85dBm power. Interferer rejection improves by an average of 9.4dB when the SA filter is enabled.

within the target attenuation bands listed in Table II. The combined filter achieves >52dB attenuation in the target frequency bands of all four SS-guided filter modes. In packet tests compliant to IEEE 802.15.4, we stimulate the receiver with RF packets and identify the power level that achieves 1% packet error rate (PER). As summarized in Table II, the receiver exceeds the sensitivity and interferer rejection requirements of both the 2450MHz and 915MHz bands. In SA filtering tests using 802.15.4 packets (Fig. 6), the receiver achieves +55dB to +63dB rejection of a +25MHz to +65MHz FM interferer when SA filtering is enabled, which averages to 9.4dB more rejection compared to when SA filtering is disabled. SA filtering achieves this improvement by detecting the FM interferer and reconfiguring the SS-guided notch filter to the mode that best attenuates the interferer.

TABLE II
SUMMARY OF PARAMETERS AND MEASUREMENTS

Technology			65nm 1P9M w/MIMCAP
Active Area			0.39mm^2
Carrier Frequency Range			600MHz to 3.4GHz
Max Gain			55.8dB
IIP3			-38dBm
SS Sweep Duration			≈121µs, 25 to 65MHz, 64 samples per bin
SS-Guided Notch Filter Mode, FIR Coefficients, and Target Attenuation Bands			1: [4 -1 4 4 -1 4], 15-23MHz 2: [2 2 4 4 2 2], 23-28MHz 3: [1 3 5 5 3 1], 28-42MHz & 58-70MHz 4: [1 3 4 4 3 1], 42 to 58MHz
SARfilter ADC FIR Filter			Tap Length: 16 to 64, Weight: 0 to 6C_{unit}
Power, 1.0V Except 0.9V Digital	Analog		6.82mW
	Digital: Controller, Notch Filter & SARfilter ADC Clocks		3.41mW, f_{conv}=5MS/s, 20-tap SARfilter ADC FIR filter 1.31mW, f_{conv}=2MS/s, 16-tap SARfilter ADC FIR filter
	LO Divider		1.94mW, 4.8GHz 2xf_{LO} 0.90mW, 1.8GHz 2xf_{LO}
	Spectrum Sensing		2.93mW
	Total		802.15.4 2450MHz band: 15.1mW 802.15.4 915MHz band excluding SS (not supported for f_{conv}=2MS/s): 9.0mW
IEEE 802.15.4 Sensitivity & Interferer Rejection		2450MHz, f_{conv}=5MS/s	-93dBm +5MHz, +30dB; +10MHz, +39dB
		915MHz, f_{conv}=2MS/s	-100dBm +2MHz, +29dB; +4MHz, +31dB

VII. CONCLUSION

We demonstrate a flexible wireless receiver that uses intelligent DT spectrum adaptive filtering to target large interferers with a reconfigurable DT notch filter. By sensing a receiver's operating environment, spectrum-sensing reduces the need to overdesign for the worst-case operating conditions. Overdesign in a conventional filter can consume two to four times more area and power.

ACKNOWLEDGEMENT

This research was supported by the U.S. Army Research Laboratory under contract W911NF and prepared through collaborative participation in the Microelectronics Center of Micro Autonomous Systems and Technology (MAST) Collaborative Technology Alliance (CTA).

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