27.6 A 90MS/s 11MHz Bandwidth 62dB SNDR Noise-Shaping SAR ADC

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In recent years, charge-redistribution SAR (Successive Approximation) ADCs have exhibited the highest conversion efficiencies for ADCs with moderate resolution and bandwidth [1-3]. For effective resolutions beyond 10b or so, however, the accuracy of the SAR circuit blocks limits the overall energy efficiency of the converter. At high resolutions, for instance, the DAC voltages become small compared to the input-referred noise of a dynamic comparator, necessitating an additional power-hungry, low-noise pre-amplifier to drive the comparator. To improve the resolutions of SAR ADCs, this work introduces a technique to decouple the accuracy of the comparator from the resolution of the ADC.

In this paper, we introduce a low-OSR (Oversampling Ratio) noise-shaping SAR ADC that leverages noise-shaping to increase the resolution of a conventional SAR ADC. The converter uses an 8b capacitor DAC and achieves an ENOB of 10.0 bits over a bandwidth of 11MHz with an OSR of 4. Through noise-shaping, we are able to mitigate some of the losses from mismatch, kT/C noise, and comparator noise by trading bandwidth for accuracy, which allows us to achieve higher resolutions using lower-resolution and lower-accuracy circuit blocks. Significantly, the input-referred noise of the comparator is noise-shaped along with the quantization noise so the comparator no longer requires the full accuracy of the converter. The noise-shaping technique presented in this paper provides a means to enhance the resolution of SAR ADCs without a significant modification to the basic SAR ADC structure.

A simplified implementation of this noise-shaping technique is shown in Fig. 27.6.1. As in a traditional SAR ADC, the input signal is first sampled onto the capacitor DAC, and the conventional binary search algorithm is performed to obtain the digital output code. As a natural consequence of this search algorithm, the DAC produces a residue voltage, which is related to the difference between the sampled input voltage and the digital output. For a typical SAR ADC, however, the DAC does not generate a residue based on the final decision, so with an additional DAC settling event following the last comparator decision, the DAC can produce a residue voltage equal to the difference between the sampled input signal and the overall digital output. This residue is then passively sampled onto another capacitor, inverted, and fed back to the inverting terminal of the comparator to provide memory into the system. A more detailed description of this process is shown in Fig. 27.6.2, which details the evolution of the DAC residue voltages over time and shows the high-pass characteristic of the resulting noise transfer function.

As shown in Fig. 27.6.1 and Fig. 27.6.2, the signal and noise transfer functions resulting from this technique resemble the transfer functions of a typical noise-shaping system. The signal transfer function describes an all-pass filter, which passes low-frequency signals, whereas the noise transfer function describes a high-pass filter, which attenuates the low-frequency components of both the quantization noise and the input-referred comparator noise within the signal bandwidth. Additionally, the digital output requires filtering to recover the desired signal bandwidth, so the high-frequency noise contributed by kT/C sampling noise and the DAC mismatch noise are filtered along with the high-frequency quantization noise, thereby reducing the white noise components of kT/C and mismatch noise.

To improve the low-frequency attenuation of the quantization noise, and increase the achievable resolution beyond that of the simplified example given in Fig. 27.6.1, the loop filter used is this design consists of a discrete-time, cascaded FIR-IIR filter. The circuit implementation of the cascaded FIR-IIR filter is shown in Fig. 27.6.3. The FIR filter is a two-tap filter constructed using two capacitor banks, where alternate DAC residue voltages are passively sampled onto the alternate capacitor banks at the end of each ADC conversion cycle. The FIR tap coefficients are set by the size of capacitors within the capacitor banks. The IIR filter is implemented with a simple, single-stage opamp, which sums and integrates the FIR filter taps onto a feedback capacitor. The FIR filter taps are summed and integrated during the sampling period of the SAR ADC, which provides sufficient time for the filter outputs to settle before the start of the next ADC conversion cycle.

The full system-level block diagram and the transfer function for the converter are presented in Fig. 27.6.4. Similar to the simplified implementation presented in Fig. 27.6.1, the full system-level transfer function indicates an all-pass signal transfer function and a high-pass noise transfer function. Although this design uses a modest two-tap FIR filter and a modest gain opamp, the low-frequency attenuation provided by the loop filter can be further improved by increasing either the number of FIR filter taps or increasing the gain the opamp, both of which will increase the converter resolution. As shown by the transfer function in Fig. 27.6.4, the attenuation provided by the noise transfer function at DC, $z = 1$, is related to the sum of the tap coefficients, α_n, and the finite gain error of the opamp, κ_A. Since the FIR filter comprised only switches and capacitors, increasing the number of FIR filter taps is an efficient means to improve the noise-shaping characteristics with minimal power increase.

The DAC consists of a differential, binary-weighted capacitor array and uses bipolar references to enable sign-magnitude encoding. The comparator is a double-differential, double-tail latch comparator [4] with one set of differential inputs connected to the output of the DAC and the other set connected to the output of the FIR-IIR filter. Similar to the simplified example from Fig. 27.6.1, this comparator configuration allows the sampled input signal to be summed with the filtered DAC residue voltage and introduces memory into the system.

The timing for this SAR ADC is generated using an asynchronous clocking scheme. A 90MHz master clock controls the sampling instance, and a single delay element is used to time each of the DAC settling events. The delay element consists of a ring oscillator with one inversion produced by a flip-flop, which when triggered by the comparator ready signal, immediately resets the comparator and initiates the inverter delays to time the DAC. By recycling a single delay element, the delays are matched between DAC settling events without the use of calibration.

The ADC is fabricated in 65nm CMOS and occupies an area of 0.0462mm^2 (231×200μm^2). The DAC is an 8b, binary-weighted capacitor array with a total differential input capacitance of 320fF. The spectral density of the converter is shown in Fig. 27.6.5 for a 2MHz input signal sampled at 90MS/s. The measured SNDR versus input frequency and input amplitude are shown in Fig. 27.6.6. The digital power consumption is 608μW, and the analog power consumption is 198μW, with 30μW for the comparator, and 45μW for the sampling circuit, 44μW for the DAC reference voltages, and 79μW for the FIR-IIR filter. With an OSR of 4, the signal bandwidth is 11MHz and the ADC achieves an ENOB of 10.0 bits with a 2MHz input signal. The FoM for this converter is 35.8fJ/conv.

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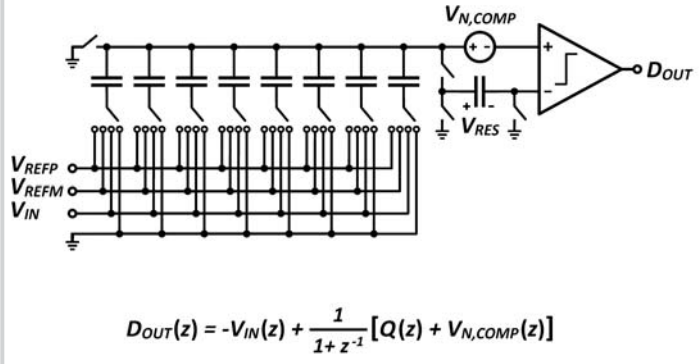

Figure 27.6.1: Conceptual scheme for introducing noise-shaping into a SAR ADC. The DAC residue is passively sampled after conversion and summed with the input during the next ADC conversion cycle through the inverting terminal of the comparator.

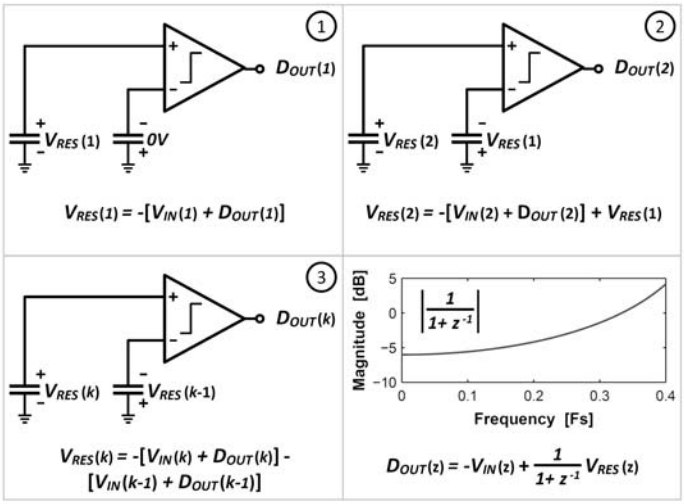

Figure 27.6.2: Time-series evolution of the DAC residue voltage from the simplified implementation in Fig. 27.6.1.

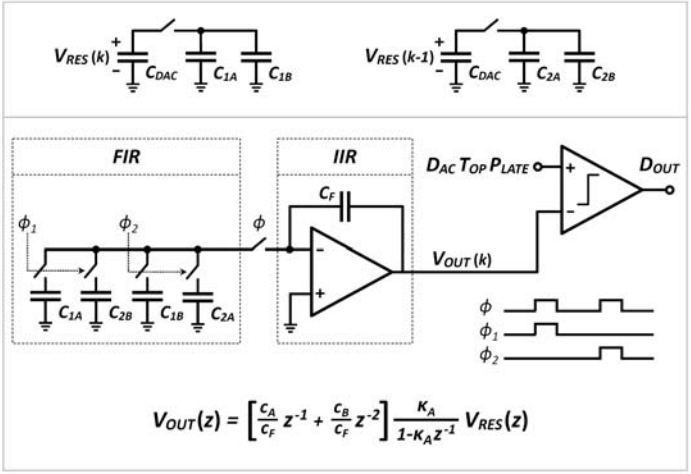

Figure 27.6.3: Circuit implementation of the discrete-time, cascaded FIR-IIR filter. The DAC residue voltages are passively sampled onto the two-tap FIR capacitor banks C_1 and C_2, which are summed and integrated in the IIR filter through the opamp.

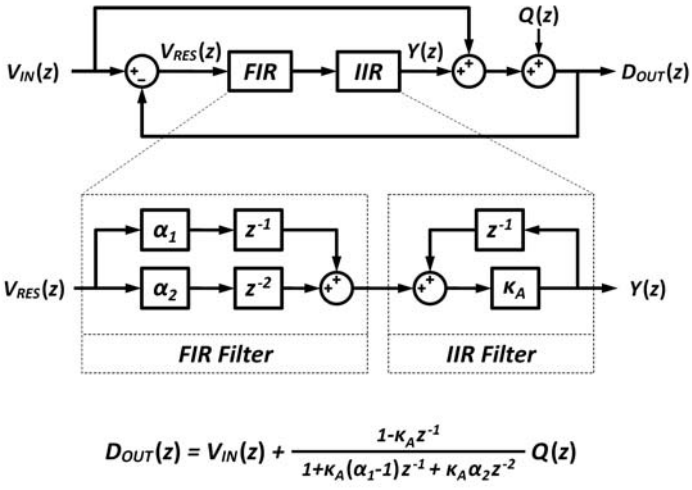

Figure 27.6.4: System-level block diagram and transfer function.

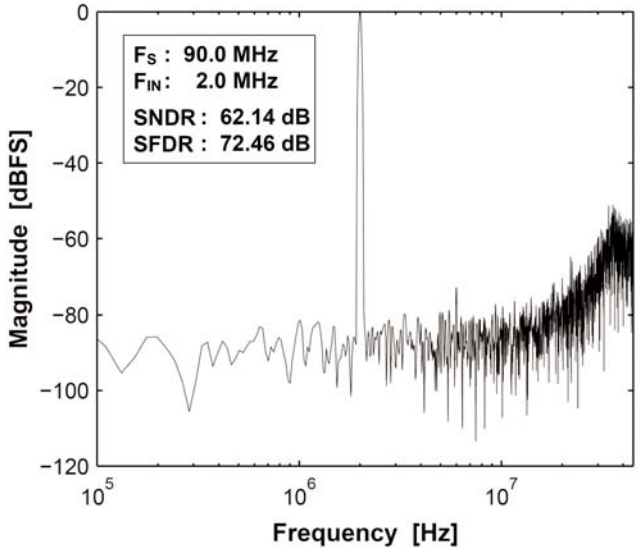

Figure 27.6.5: Output spectrum from a 4096-point FFT.

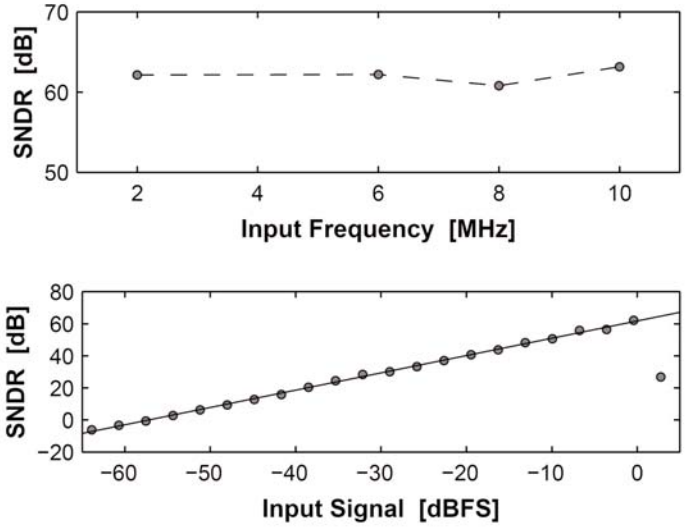

Figure 27.6.6: Convertor SNDR characteristics.

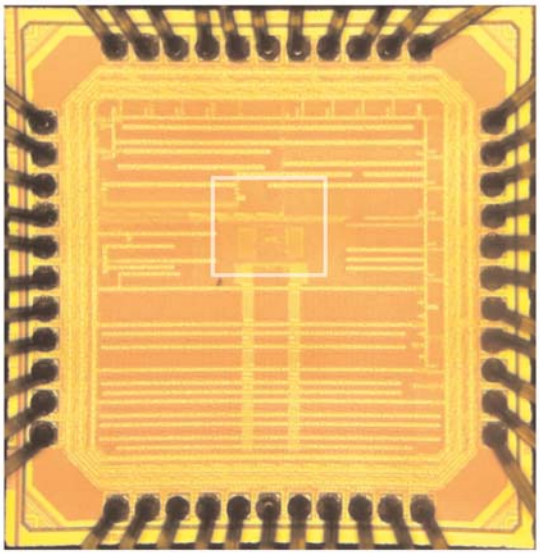

Figure 27.6.7: Die micrograph. 231µm X 200µm Active Area.

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