

A 1.5-GS/s Flash ADC With 57.7-dB SFDR and 6.4-Bit ENOB in 90 nm Digital CMOS

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Abstract—A 7-bit 1.5-GS/s analog-to-digital converter (ADC) incorporates redundancy, reassignment, and digital correction to reduce the complexity of analog functions and the required accuracy compared to traditional Flash ADCs. Deliberate and random mismatch is used to set the desired trip points, achieving a 600-mV_{pp} differential input signal range. The need for a low-impedance high-precision resistor reference ladder is eliminated, and comparator performance is decoupled from matching requirements, so that small and fast dynamic comparators can be used. New analysis discusses the optimum combination of random and deliberate comparator offset to achieve a target effective number of bits (ENOB). This prototype ADC has the highest ENOB and highest sampling frequency of any reported Flash ADC utilizing redundancy. A proof-of-concept prototype achieves no missing codes, 46.6-dB spurious-free dynamic range, and 6.05-bit ENOB at Nyquist input frequency. Fabricated in 90-nm digital CMOS, with a core area of 1.2 mm², the device consumes 204 mW from a 1.2-V/0.9-V analog/digital supply.

Index Terms—Digital calibration, Flash analog-to-digital converter (ADC), mismatch, reassignment, redundancy.

I. INTRODUCTION

FOR FLASH ADCs, the bandwidth–accuracy–power trade-off becomes more stringent in finer linewidth technologies, because this relationship is determined by process-dependent parameters [1] that characterize transistor matching. Unlike conventional designs, this work exploits the effects of V_T mismatch. The accuracy requirements for comparators can be significantly relaxed, allowing the ADC design to leverage the benefits of digital scaling. In [2]–[4], a comparator redundancy scheme is introduced to decouple performance from matching requirements. We advance this technique by employing random and deliberate mismatch to set the desired trip points of the comparators and thus eliminate the need for a low-impedance high-precision resistor ladder. Unusually, the proposed technique exploits large random variation in comparator offset. This enables the use of low-precision dynamic comparators that can be optimized for speed.

Section II presents an outline of the ADC architecture. Section III discusses the implementation of the key blocks. A challenge in this design is to achieve large random variation in comparator offset and, at the same time, satisfy the input-referred noise requirement of the comparators. Section IV considers this tradeoff and the implications for energy efficiency

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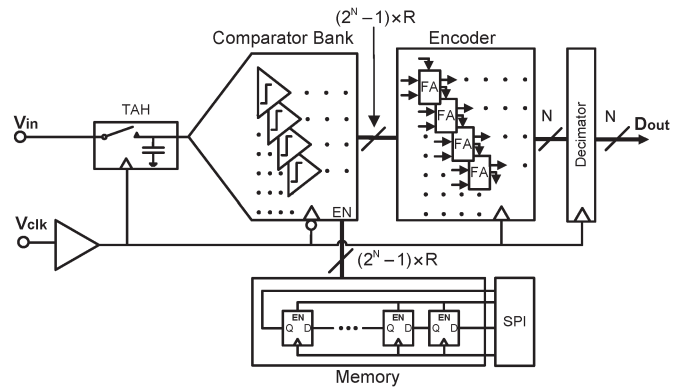


Fig. 1. N -bit ADC architecture with a redundancy of R comparators per code. $(2^N - 1) \times R$ refers to the number of comparators in the comparator bank and dictates the number of comparator output and comparator enable signals.

of the comparator. Measurement results and conclusion are presented in Sections V and VI, respectively.

II. ARCHITECTURE

Fig. 1 shows a block diagram of the proposed ADC architecture. A track-and-hold (TAH) circuit samples a differential input signal (single-ended shown), which is subsequently processed by a subset of a bank of redundant comparators. No reference ladder is required since the comparator trip points are set by a combination of deliberate and random mismatch. At startup, a calibration routine finds the comparators closest to the desired trip points. Sufficient redundancy ensures that enough variation exists about a predefined set of deliberate mismatches to ensure that the comparator bank spans the desired input range. Furthermore, because this technique decouples comparator performance from matching requirements, the comparators can be made small and fast. Only useful comparators are enabled. Each comparator can be independently enabled or disabled, and a memory element associated with each comparator stores the comparator ON/OFF states. The memory elements are serially connected, forming a memory block that is accessible through a serial peripheral interface. An encoder block, comprising full adders, resolves the comparator outputs to the 7-bit ADC output code.

III. IMPLEMENTATION

A. Comparator Bank

The comparator bank incorporates redundancy¹ and reassignment to correct differential nonlinearity (DNL) errors [2],

¹The term “redundancy” in this work refers to the number of comparators available per code where the most suitable comparators are selected at power-on. Unselected comparators remain powered off.

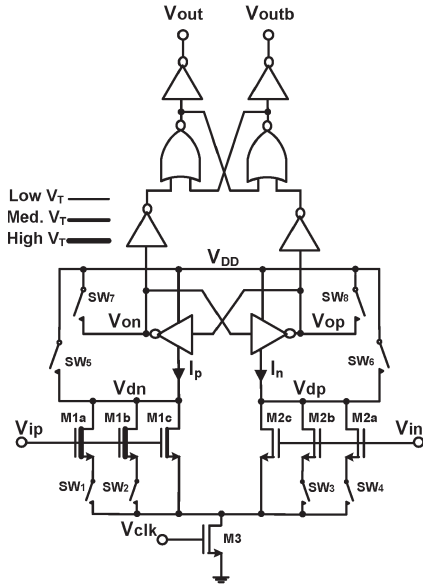


Fig. 2. Comparator circuit with programmable offset.

[3]. A conservative value of ten was chosen for comparator redundancy in this proof-of-concept design. In this scheme, multiple redundant comparators are assigned to each code to increase the probability of finding a comparator with a trip point close to each ideal trip point. Furthermore, by allowing comparators with large random offsets, which were originally designated to specific codes, to be reassigned to more suitable codes, offset do not compromise ADC accuracy, regardless of their magnitude.

Since this ADC architecture does not employ a resistor ladder, comparator thresholds are determined by a combination of deliberate and random offsets. Random offsets alone would limit the dynamic range of the ADC. This is because large random offsets require small devices, which, in turn, leads to higher noise, degrading SNR. Therefore, deliberate offsets are introduced to the comparators to increase dynamic range. Increasing the dynamic range increases the LSB size for a given resolution, therefore improving SNR. The minimum input range is dictated by the input-referred noise value that allows the ADC design to meet a target SNR. On the other hand, it is also necessary that random offsets adequately cover the desired range between deliberate offsets, and this limits the maximum input range. In Section IV, we show that only a small number of deliberate offsets need to be introduced.

B. Comparator

The comparator, based on [5], is modified to introduce a deliberate offset. This current latch sense amplifier, as shown in Fig. 2, leverages small devices for power and speed, and also exhibits large offsets suited for redundancy and reassignment. Deliberate offsets are introduced by asymmetric sizing of the input pair and by the use of field-effect transistors (FETs) with differing threshold voltages. The input differential pair of the comparator is formed as composite devices M1a-c and M2a-c. M1a-c and M2a-c are formed by combinations of low, medium, and high V_T devices. The use of devices with different threshold voltages for the input pair limits the amount of asymmetrical sizing needed for a given offset. Different V_T combinations are

assigned to different comparators during layout. Furthermore, asymmetric sizing is introduced with switches SW1–SW4, which hardwire the programming of the widths of the input pair. A standard unit cell (Fig. 2) is used to implement all comparators in the comparator. This allows programming of the deliberate offsets to be achieved with automated schematic design, layout, and simulation. Increasing the input range by adding branches to the composite devices M1–M12 of the comparator in Fig. 2 increases the input capacitance of the comparator bank and puts a heavier burden on the input sampling switch for a given settling time requirement. Therefore, comparator input capacitance, along with noise and offset, dictate the input range, and 600 mV_{DD} was found to be optimal.

The comparator, including the SR latch, buffers, and enable/disable functionality, occupies an area of $100 \mu\text{m}^2$, of which 30% is the input FETs, SW1–SW4, and M3.

The circuit operation is given as follows: When V_{clk} is low, all internal nodes including V_{dn-p} and V_{op-n} are preset to V_{DD} by switches SW5–SW8. When V_{clk} goes high, the input pair senses input voltages V_{ip} and V_{in} and induces differential currents I_p and I_n through M1a–c and M2a–c, respectively. The current difference is converted to a large voltage difference through regeneration and latching of the cross-coupled inverters at nodes V_{op-n} . The final output voltage difference $V_{op} - V_{on}$ reaches $\pm V_{DD}$ and is subsequently latched by an SR latch to retain the decision during the reset phase.

C. Boot-Strapped TAH

A TAH circuit is used to reduce the jitter requirements for the comparator sampling clock and to minimize the effects of skew in the clock path of the comparator bank. The TAH circuit consists of an n-channel metal–oxide–semiconductor (MOS) switch and a hold capacitor, which comprise the routing capacitance and the input capacitance of the comparator bank. Furthermore, the TAH is bootstrapped [6] in order to operate at a 1.2 V supply and to reduce signal dependence.

D. Encoder

The outputs of all the comparators are routed to an encoding block and summed to form a 7-bit output word. Addition permits comparators to be easily reassigned to any code and eliminates nonmonotonicity. The encoder uses a Wallace tree architecture [7], in combination with carry-select adders and pipelining, to resolve the comparator outputs at 1.5 GS/s. This encoding scheme is inherently independent of the comparator assignment, since it adds the number of logic highs present at its input. Furthermore, since only 127 comparators are enabled after calibration and disabled comparators do not contribute to the encoded result, 7-bit encoding is guaranteed.

E. Calibration Algorithm

At power-on, an off-chip calibration engine initiates a comparator search algorithm [4]. With the aid of an off-chip digital-to-analog converter (DAC), input voltages spanning the desired trip voltages are applied to the input of the comparator bank to search for the optimum comparator to assign to each code. During the search, the calibration engine enables a trial comparator. Comparators that have already been selected during

earlier searches are also enabled. This mimics the effects of comparator kickback seen during normal operation and minimizes any differences between IR drops on the supply lines during calibration and normal operation. The calibration engine then instructs the DAC to sweep the input voltage about the desired trip voltage. If the trial comparator is suitable, its output will toggle, causing the output of the encoder to transition between X and $X - 1$, where X is the total number of comparators enabled. For a 7-bit ADC, the search finishes when 127 (i.e., $2^7 - 1$) comparators are selected. Unselected comparators remain powered off.² Finally, it should be noted that the input range is set by the maximum deliberate comparator offset and is hardwired into the design. Sweeping the calibration DAC beyond this input range reduces the effectiveness of random comparator offset and degrades DNL.

IV. COMPARATOR ANALYSIS

A challenge in the design of the comparators is to achieve a large random variation in offset, which is beneficial for redundancy and reassignment, and, at the same time, to satisfy the input-referred noise requirement. This design employs small low-precision comparators with large random offsets approximated by [8]

$$\sigma_{\text{comp}} \approx \frac{A_{V_T}}{\sqrt{WL}} \quad (1)$$

where A_{V_T} is the V_T mismatch coefficient, and W and L are the width and length of the comparator input differential pair, respectively. Equation (1) shows that the use of small devices results in a large random offset, which, in turn, enables a wider distribution of trip voltages for the redundancy and reassignment scheme. However, the use of small devices also tends to increase the input-referred noise of the comparators, which, in turn, limits the ADC SNR. In [9], it is shown that thermal noise from the input pair and kT/C noise from switches SW7–SW8 during reset are the dominant sources of noise. To first order, the input-referred noise equivalents of these sources, which were validated with Spectre transient noise simulations, are given by [9]

$$\overline{\delta v_{\text{eq_M1-M2}}^2} \approx \frac{2kT\gamma \cdot v_{\text{dsat1}}}{C_d V_{\text{TN}}} \quad (2)$$

$$\overline{\delta v_{\text{eq_SW7-SW8}}^2} \approx \frac{kT \cdot v_{\text{dsat1}}^2}{2C_o V_{\text{TN}}^2} \quad (3)$$

where v_{dsat1} is the overdrive voltage of the input pair; V_{TN} is the threshold voltage of the n-channel FETs of the cross-coupled inverter pair, γ is the MOS noise factor; and C_d and C_o are the capacitances at nodes $V_{\text{dn-p}}$ and $V_{\text{op-n}}$, respectively. Equations (2) and (3) show that increasing the capacitance at nodes $V_{\text{dn-p}}$ and $V_{\text{op-n}}$ or reducing v_{dsat1} by increasing the widths of the input pair, reduces noise.

Fig. 3 plots comparator input-referred offset and noise versus device width, using data obtained from Spectre simulations. The x -axis is the width of M1–M3 and of the cross-coupled in-

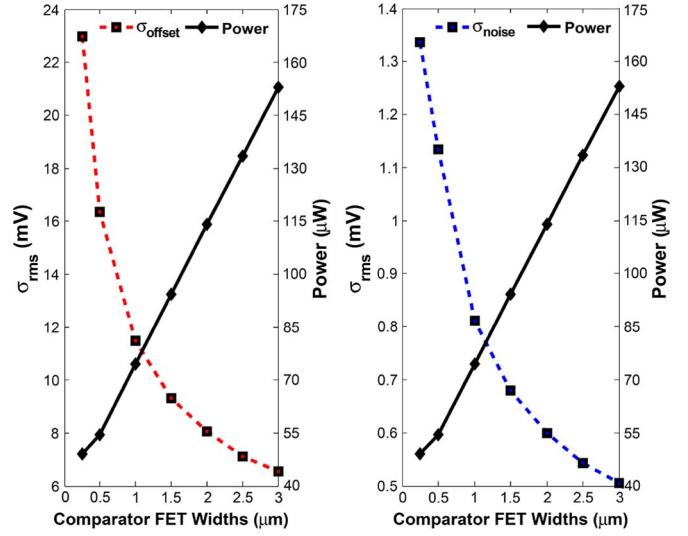


Fig. 3. Spectre simulated comparator (a) offset, (b) noise, and (a) and (b) power (at 2 GHz and 1-V V_{DD}) versus comparator FET widths for M1–M3 and cross-coupled inverters of the comparator in Fig. 2.

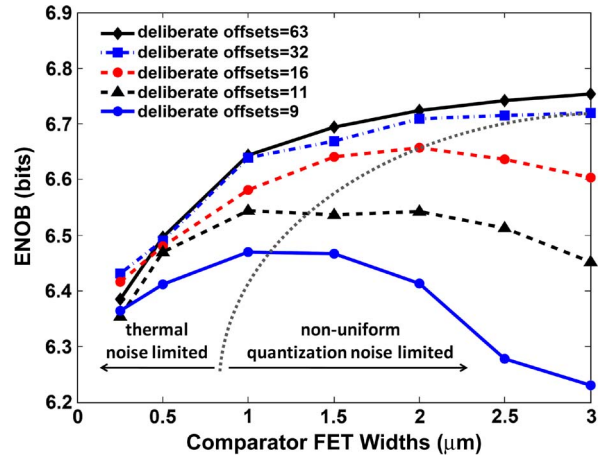


Fig. 4. Monte Carlo simulation of ENOB versus FET widths for 7-bit ADCs using data from Fig. 4 and a redundancy of 5.

verters of the comparator in Fig. 2.³ The comparator is clocked at 2 GHz, and the circuit uses a 1-V V_{DD} . Power is plotted alongside noise and offset to illustrate the tradeoff between power, offset, and accuracy. Fig. 3(a) shows the advantages of small width in terms of power consumption and increased spread of input offset, which is beneficial for comparator redundancy and reassignment. On the other hand, Fig. 4(b) shows that the input-referred noise also increases for small transistor widths. Fig. 4 illustrates a tradeoff between noise and offset that is unique to the proposed ADC architecture. The use of large device widths results in lower noise, which improves ADC SNR but also reduces comparator random offset. A smaller random offset requires the ADC to utilize more deliberate offsets, compensate for the lack of spread from random offset, and achieve sufficiently small granularity for a given dynamic range. In doing so, the amount of SNR degradation due to

²The clock input to each comparator is preceded by a series switch that disconnects the local clock buffer to any disabled comparator.

³These simulations consider composite devices M1a,b,c and M2a,b,c as single nominal V_T devices. Switches SW5–SW8 are sized to ensure adequate reset functionality at 2 GHz for each point in Fig. 4. Switches SW1–SW4 are not included.

both thermal noise and nonuniform quantization noise can be minimized but at the expense of increased complexity in comparator design. The choice of device dimensions therefore depends on the target ADC SNR and the number of deliberate offsets employed.

Fig. 4 shows a plot of the effective number of bits (ENOB) of a 7-bit Flash ADC versus the comparator device widths. The data are generated by a Monte Carlo model of a bank of comparators with a redundancy of five comparators per code and with the most suitable comparator selected for each code. The offset and noise data from Fig. 3 are used in this model. Each data point in Fig. 4 is the average ENOB observed for 100 randomly generated ADCs, and each of the five curves corresponds to a different number of deliberate offsets employed. For small device widths, the plot shows a low ENOB that is largely independent of the number of deliberate offsets used. A low ENOB at small device widths indicates that ADC performance is dominated by thermal noise. On the other hand for large widths, insufficient random variation in offset results in fewer trip voltages between deliberate offsets, so that ENOB degradation from nonuniform quantization dominates. This effect is more apparent for ADCs employing a small number of deliberate offsets.

For a given target ENOB, there exists an optimum combination of the number of deliberate offsets and comparator device size. Fig. 3 shows that increasing the comparator device widths to mitigate noise and random offset also increases power consumption. Furthermore, Fig. 4 shows that, for a given number of deliberate offsets, there exists a device width that maximizes ADC ENOB. Beyond this point, the power consumption increases with increased device width and unlike traditional Flash ADCs, the ADC accuracy for the proposed architecture degrades. This is because there is no longer a large-enough random variation in comparator offset to cover the gap between deliberate offsets, causing an increase in quantization noise.

As an example, for device widths of $1\ \mu\text{m}$, Fig. 4 shows that there is sufficient random variation in comparator offset to require only 16 deliberate offsets to achieve an average ENOB of 6.58 bits. Simulations also indicate that 90% of the ADCs achieve an ENOB that is greater than 6.5 bits. Increasing device widths up to $2\ \mu\text{m}$ further improves ENOB but also increases power consumption. Beyond $2\ \mu\text{m}$, as shown in Fig. 4, ADC ENOB degrades because of increasing nonuniform quantization noise. In conclusion, for a target ENOB, there exists an optimum combination of the number of deliberate offsets and comparator device size that minimizes design complexity and power.

V. MEASUREMENT RESULTS

The prototype, which was fabricated in a 90-nm digital CMOS process, occupies a core area of $1.2\ \text{mm}^2$. A die micrograph is shown in Fig. 5. The prototype is tested as a chip-on-board device to reduce the effects of bond-wire inductance. The prototype ADC has a differential input signal range of $600\ \text{mV}_{\text{pp}}$ and 700-mV common mode.⁴

⁴The common mode is set by a single off-chip ADC driver that conditions the input signal from both the test equipment and off-chip calibration DAC. This eliminates any common-mode variation between normal operation and calibration.

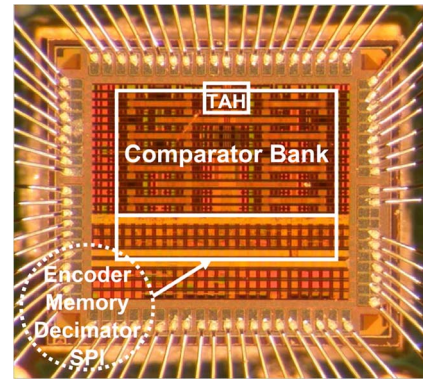


Fig. 5. Die micrograph of 90-nm CMOS ADC.

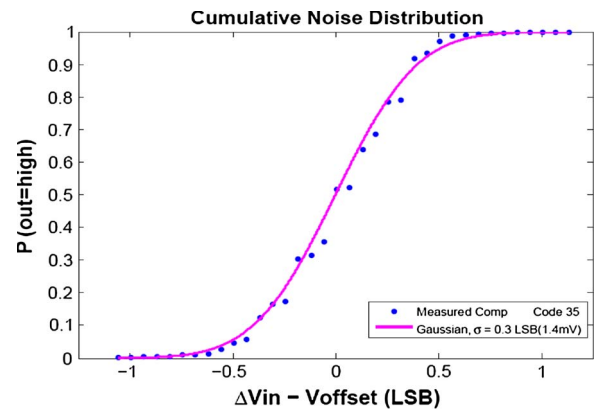


Fig. 6. Experimental data on comparator cumulative noise distribution and Gaussian fit.

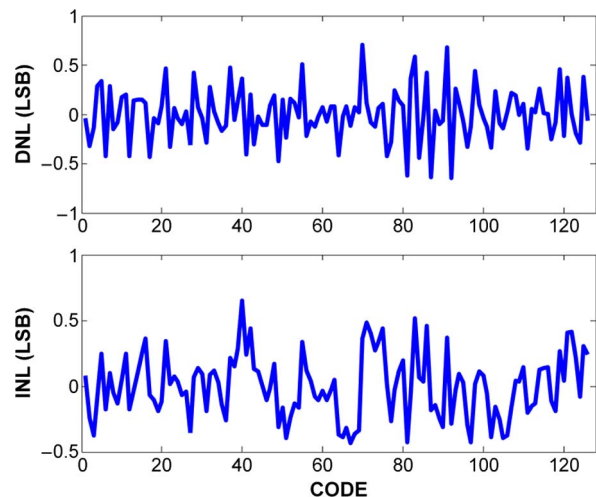


Fig. 7. Measured DNL and INL.

Fig. 6 shows the experimentally measured input referred noise of the proposed comparator. The equivalent input noise is determined by sweeping a differential voltage at the ADC input about a comparator's threshold and averaging the number of logic ones. The data are fitted to a Gaussian distribution. The measurements show $0.3\ \text{LSB}$ of the input-referred RMS comparator noise.

The maximum measured DNL/integral-nonlinearity values are $0.70/0.64\ \text{LSB}$ (Fig. 7). Fig. 8 shows a 4096-point

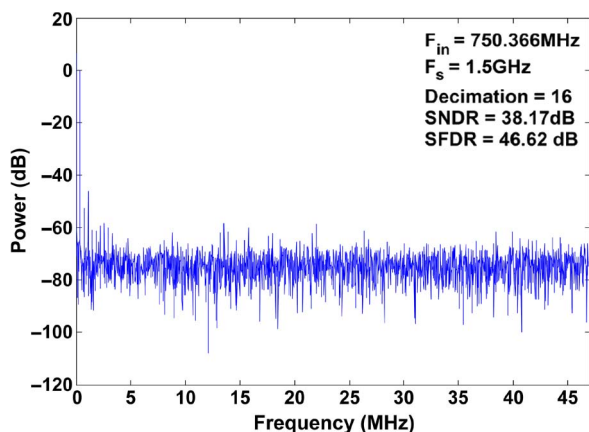


Fig. 8. FFT of 4096 points for 750.36-MHz input and 16× decimation.

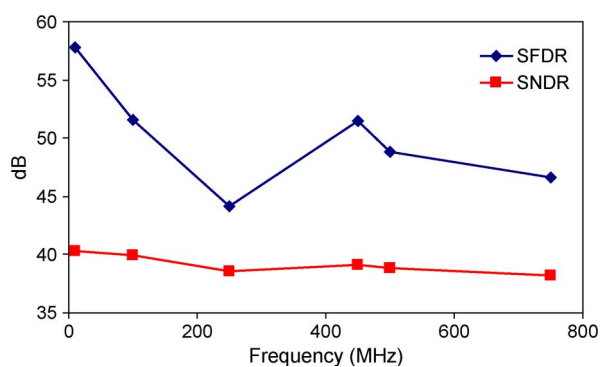


Fig. 9. SNDR and SFDR versus F_{in} ($F_s = 1.5$ GS/s).

TABLE I
COMPARISON WITH RECENT FLASH ADCs LEVERAGING DEVICE MISMATCH

| Reference | F_s (GS/s) | F_{in} (MHz) | ENOB (bits) | SFDR (dB) | PWR (mW) |
|-----------|--------------|----------------|-------------|-----------|----------|
| This work | 1.5 | 750 | 6.05 | 46.6 | 204 |
| [10] | 1.5 | 750 | 5.44 | 43 | 35 |
| [11] | 0.008 | 1 | 5.29 | 42.86 | 0.631 |
| [12] | 0.0004 | 0.2 | 5.1 | 39.1 | 0.002 |

fast Fourier transform spectrum for an input frequency of 750.4 MHz sampled at 1.5 GHz.⁵ Fig. 9 shows the measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) as a function of the input frequency at 1.5 GS/s. The ADC achieves an ENOB and SFDR of 6.4 bits and 57.7 dB at low frequency, respectively, and 6.05 bits and 46.6 dB at Nyquist, respectively. There is no measurable degradation in SNDR over 24 h of operation, and the measured BER at 1.5 GS/s is less than 2.7×10^{-15} . The ADC consumes a total of 204 mW at Nyquist from 1.2 V analog and 0.9 V digital supplies. The comparator bank and repeaters, TAH and clock buffers, and encoder consume 23%, 25%, and 52% of the power, respectively. Table I shows a comparison with recent Flash ADCs that leverage device mismatch.

⁵The output data are decimated by 16× for reliable transmission off-chip. Decimation also explains why the near-Nyquist tone leads to a low bin number fundamental in Fig. 8.

VI. CONCLUSION

This brief has proposed a 7-bit 1.5-GS/s Flash ADC with comparator trip points set purely by random and deliberate mismatch. A calibration algorithm at power on sweeps a 600-mV_{PP} differential input to select the most suitable subset of a bank of redundant comparators. Unselected comparators are powered off. Power consumption is dominated by the encoding and clock network, which consume 77% of the 204 mW of total power. The conservative value of comparator redundancy in the prototype doubles the complexity of both the clock wiring and encoder. Extensive pipelining in the encoder to achieve very low measured BER also increases power consumption. However, this architecture scales with CMOS technology and benefits from the power and speed advantages associated with each new process node. The proposed technique eliminates the need for a low-impedance high-precision resistor ladder. Furthermore, comparator bandwidth and accuracy requirements are decoupled, so that small and fast dynamic comparators, which are amenable to digital scaling, can be used. The prototype ADC has the highest ENOB and highest sampling frequency of any reported Flash ADC utilizing redundancy.

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REFERENCES

- [1] K. Uyttenhove and M. S. Steyaert, "Speed-power-accuracy tradeoff in high-speed CMOS ADCs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 4, pp. 280–287, Apr. 2002.
- [2] C. Donovan and M. P. Flynn, "A 'digital' 6-bit ADC in 0.25- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 432–437, Mar. 2002.
- [3] M. P. Flynn, C. Donovan, and L. Sattler, "Digital calibration incorporating redundancy of flash ADCs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 5, pp. 205–213, May 2003.
- [4] I. Bogue and M. P. Flynn, "A 57 dB SFDR digitally calibrated 500 MS/s folding ADC in 0.18 μ m digital CMOS," in *Proc. IEEE CICC Dig. Tech. Papers*, 2007, pp. 337–340.
- [5] T. Kobayashi, K. Nogami, and T. Shirotori, "A current-controlled latch sense amplifier and static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, Apr. 1993.
- [6] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
- [7] F. Kaess, R. Kanan, B. Hochet, and M. Declercq, "New encoding scheme for high-speed flash ADCs," in *Proc. IEEE ISCS*, 1997, pp. 5–8.
- [8] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.
- [9] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.
- [10] J. Proesel, G. Keskin, J.-O. Plouchart, and L. Pileggi, "An 8-bit 1.5 GS/s flash ADC using post-manufacturing statistical selection," in *Proc. IEEE CICC Dig. Tech. Papers*, Sep. 2010, pp. 1–4.
- [11] S. Weaver, B. Hershberg, D. Knierim, and U.-K. Moon, "A 6b stochastic flash analog-to-digital converter without calibration or reference ladder," in *Proc. IEEE ASSC Dig. Tech. Papers*, 2008, pp. 373–376.
- [12] D. Daly and A. Chandrakasan, "A 6b 0.2-to-0.9 V highly digital flash ADC with comparator redundancy," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 554–635.