

A 2.4GHz 2Mb/s Digital PLL-based Transmitter for 802.15.4 in 130nm CMOS

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Abstract — A fully integrated 2.4GHz transmitter for 802.15.4 based on a digital $\Sigma\Delta$ fractional- N PLL is presented. A self-calibrated two-point modulation scheme enables modulation rates much larger than the loop bandwidth. An oversampled 1-bit quantizer is used as a phase detector, reducing spurs and nonlinearity associated with some TDC-based digital PLLs. The prototype achieves an MSK modulation rate of 2Mb/s, delivers -2dBm of output power, and is free of in-band fractional spurs. The transmitter, implemented in 130nm CMOS, consumes 17mW from a 1.2V supply and occupies an active area of 0.6mm².

Index Terms — Delta-sigma, fractional- N , MSK, phase-locked loop, synthesizer.

I. INTRODUCTION

The IEEE802.15.4 standard specifies a 2.4GHz PHY that uses O-QPSK modulation with half-sine pulse shaping. This modulation is equivalent to MSK and MSK transmitters are typically implemented using Cartesian or fractional- N PLL-based modulators. Cartesian transmitters use in-phase and quadrature paths requiring DACs, low-pass filters, and RF mixers. These tend to be power hungry and the use of analog components makes this approach unsuitable for nanometer CMOS processes.

Although many 2.4GHz band transmitter/PLL designs are reported [1-4], most have some limitations. [1,2] are based on analog fractional- N PLLs and use components such as charge pumps and analog low pass filters, making them less suitable for nanometer CMOS. Although [3] employs a digital fractional- N PLL, it suffers from fractional spurs due to nonlinearity and finite resolution of the time-to-digital converter (TDC). Furthermore, TDC-based digital PLLs require extensive calibration of delay elements to reduce spurs. A digital PLL similar to this work is reported in [4], but has a relatively slow modulation rate and low output power level.

In this paper, a digitally-dominant $\Sigma\Delta$ fractional- N PLL-based transmitter achieves an MSK modulation rate of 2Mb/s. A compact PA that does not require an output matching network delivers -2dBm of output power to a 50 Ω load. The prototype transmitter is largely comprised of synthesized digital logic and the only analog components

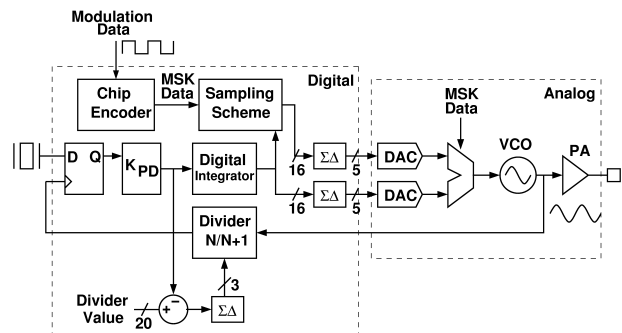


Fig. 1. The prototype 802.15.4 transmitter.

are a VCO, two DACs, and a multiplexer. An oversampled one-bit phase quantizer is used instead of a TDC as a phase detector. Because the phase detector is formed with a single flip-flop, it does not require calibration of delay elements and is more linear therefore reducing spurs associated with the use of multi-bit TDCs. Furthermore, a high reference frequency places the fractional spurs out of band. A self-calibrated two-point PLL modulation scheme allows modulation rates that far exceed the loop bandwidth.

Section II introduces the transmitter architecture. The phase detector operation is explained in Sec. III. Section IV elaborates on the modulation scheme and Sec. V covers the design of the PA. Implementation details and test setup are given in Sec. VI followed by measurement results in Sec. VII. Finally, Sec. VIII concludes the paper.

II. TRANSMITTER ARCHITECTURE

Figure 1 shows a block diagram of the prototype transmitter. The transmitter is comprised of a mostly-digital fractional- N PLL modulator and a two-stage power amplifier. A digital phase detector (PD) compares the reference clock and the divided-down VCO output. A digital integrator averages the PD output. This averaged output sets the VCO varactor voltage. The output of the integrator is converted to the analog domain by a resistor string $\Sigma\Delta$ DAC. As explained later, two control paths, incorporating two DACs and a digital sampler, enable a

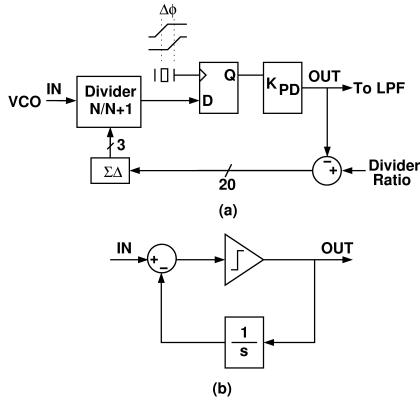


Fig. 2. (a) The digital phase detector. (b) A delta modulator.

self-calibrated two-point modulation scheme. A two-stage PA delivers an output power of up to -2dBm to a $50\ \Omega$ load. A programmable divider is controllable from 8 to 15. A second order $\Sigma\Delta$ modulator controls the divider.

III. PHASE DETECTOR OVERVIEW

Figure 2(a) shows a block diagram of the phase detector first presented in [4]. A single flip-flop oversamples the phase difference, $\Delta\phi$, between the reference and the divided down VCO. The quantized phase information is also fed back to the input of the $\Sigma\Delta$ divider to keep the phase difference between the reference and divider output small. The operation of this feedback loop is similar to that of a delta modulator (Fig. 2(b)) which consists of a feedback loop with a quantizer in forward path, and an integrator in the feedback path. Integration in the feedback path is achieved by feeding quantized phase information back to the frequency control of the divider. The delta modulator helps keep $\Delta\phi$ smaller than one quantization step. The quantization noise from the fractional- N $\Sigma\Delta$ modulator of the divider acts as dither for the oversampled phase quantizer. The integrated output (digital) of the phase detector is a digital word equal to the phase difference between reference clock and divided down VCO.

IV. FREQUENCY SWITCHING SCHEME

MSK modulation is a form of FSK with frequency deviation of $1/(2T_C)$. For 802.15.4, the bit period T_C is $1/(2\text{MHz})$ giving a frequency deviation of 500kHz relative to the channel frequency. A two-point self-calibrated frequency-switching modulation scheme enables modulation rates much higher than the PLL bandwidth. A block diagram of the frequency-switching scheme is shown in Fig 3(a) [4]. VCO control is split into two paths, one

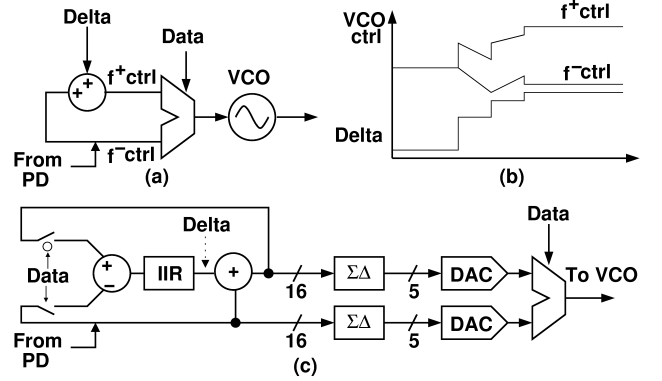


Fig. 3. (a) The two-point frequency modulation scheme, (b) an example of settling behavior, and (c) detail of modulation scheme.

path for each frequency f^+ and f^- . During each bit period the loop attempts to settle to either f^+ or f^- . At the end of each bit period, the digital value of the VCO control is sampled. The difference, *delta*, between the control word for f^+ and f^- , is calculated and updated. This difference, *delta*, is added to the VCO control for frequency f^+ to give an initial VCO control value for frequency f^- . As the modulation continues to switch between f^+ and f^- , the estimate of *delta* converges to the correct VCO input difference for the required frequencies f^+ and f^- . When *delta* converges, then to a first order, the frequency switching rate is no longer dependent on the settling time of the PLL because the correct input to the VCO is readily applied for each frequency change. An example of settling behavior is shown in Fig. 3(b), where after some data transitions, accurate VCO control inputs for the two frequencies are determined. Figure 3(c) shows a more detailed block diagram of the modulation scheme. A digital IIR filter averages the difference between f^+ and f^- and two control paths for the VCO are formed with $\Sigma\Delta$ resistor string DACs. An analog multiplexer switches between the two VCO control voltages generated by the DACs at each data transition.

V. POWER AMPLIFIER

Figure 4 depicts the power amplifier used in this work. The PA is comprised of two stages. The first stage is an inverter amplifier with resistive feedback. Because of the feedback resistor R_f , the first stage of the PA is self-biased. Linearity is improved as the bias point of the first stage is set at the middle of the analog (high gain) swing range. The input resistance of the first stage is approximated by $R_{in} \approx 1/(gm_1 + gm_2)$, and the first stage is sized to have a large input resistance to avoid loading the VCO. The second stage is sized to deliver 0dBm to a $50\ \Omega$ load.

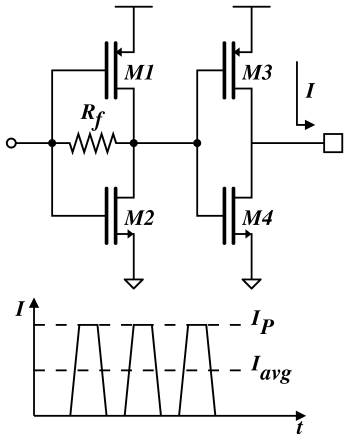


Fig. 4. The two-stage resistor feedback inverter-based PA.

There are no internal/external matching circuits or inductors used in this PA yielding a compact area. The PA efficiency is defined as the output power divided by average DC power given by (1) where I_{avg} is estimated to be half of I_P , the peak current delivered to the load. The PA is designed to have a 0dBm output power with simulated efficiency of 17%.

$$PA \text{ efficiency} = \frac{P_{out}}{P_{DC}} \approx \frac{I_P^2 R_L}{V_{DD} \cdot I_{avg}} \quad (1)$$

VI. IMPLEMENTATION DETAILS AND TEST SETUP

The prototype transmitter (Fig. 5) is implemented in 130nm mixed-mode CMOS and occupies an active area of 0.6mm^2 , and a total area of 2mm^2 including pads. The device is packaged in a 32-pin QFN package. The $\Sigma\Delta$ modulators, the LPFs, the modulation scheme and chip encoder are implemented as synthesized logic and occupy 0.07mm^2 , which is a small fraction of the overall area.

The VCO is tuned to 2.405GHz using digital switches, which add or remove VCO capacitances. A reference clock of 200MHz is used, with a nominal output frequency of 2.405GHz, which corresponds to a division ratio of 12.025. The phase detector gain K_{PD} is set to 0.01, and the loop filter gain is set to 0.03, resulting in a loop bandwidth of 145KHz. The LC VCO has an NMOS cross-coupled pair and a PMOS current source. The simulated VCO gain is 25MHz/V. The VCO gain is kept small in order to prevent the DAC quantization noise from corrupting the output phase noise. A high reference clock is required, so that the phase quantizer adequately over-samples the phase information. In order to convert from the digital to analog domain, a first order $\Sigma\Delta$ modulator controls a 5-bit resistor-string DAC. The programmable divider is referenced in [4], where each of the 2/3 divider cells are identical. The division ratio is controllable from 8 to 15.

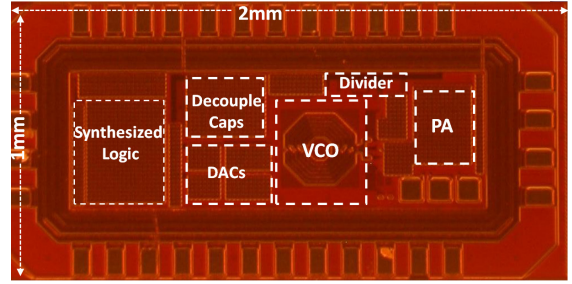


Fig. 5. Die photo.

802.15.4 packets are generated in an FPGA. The modulation chip sequence is then sent to the prototype device for transmission. An on-chip encoder converts the O-QPSK chip codes to MSK equivalents. The output of the transmitter is demodulated using a TI CC2420 evaluation board for verification. Output spectrum is measured with an Agilent E4405B spectrum analyzer.

VII. MEASUREMENT RESULTS

Figure 6 shows the measured output spectrum of the PLL without modulation. The measured output power at 2.405GHz is -2dBm. Figure 7 shows the MSK spectrum when a 2Mb/s PRBS modulation data is applied to the PLL through the FPGA. The IEEE 802.15.4 mask requirements are fulfilled. Multiple packets are successfully demodulated using the CC2420 evaluation board. Although the PLL loop bandwidth is only 145KHz, the self-calibrated two-point modulation scheme enables modulation at rate of 2Mb/s. Figure 8 shows the measured phase noise of the PLL. The phase noise at 3.5MHz offset is -120dBc/Hz which meets the 802.15.4 requirement. The PLL is free of in-band fractional spurs. The closest measured fractional spur is -60.2dBc at 5MHz offset. Figure 9 shows the trellis diagram of the PLL for 2Mb/s MSK modulation.

The synthesized logic uses 4mA. At -2dBm output power, the PA consumes 4.5mA. Current consumption of 5.7mA is attributed to the divider, the VCO, and the DACs. The total power consumption of the transmitter is measured to be 17mW with 12.5mW attributed to the PLL. The chip operates with an analog and digital supplies of 1.2V. The performance of the transmitter is summarized and compared to some recent papers in Table 1.

VIII. CONCLUSION

This paper presents a fully integrated 2.4GHz transmitter in 130nm CMOS that meets the requirements of 802.15.4 standard. The $\Sigma\Delta$ fractional-N PLL is

TABLE I
COMPARISON WITH PRIOR ART

Ref	Tech/VDD CMOS	PA o/p	Modulation Rate/Type	Output Frequency	Power consumption (PLL/PA)	Phase Noise @3.5MHz offset	Core Area
This	130nm/1.2V	-2dBm	2Mb/s MSK	2.4-2.5 GHz	12.5/4.5 mW	-120dBc/Hz	0.6mm²
[1] ISSCC 09	180nm/1.8V	4dBm	2Mb/s GMSK	2.48GHz center	13.32/16.39 mW	-126dBc/Hz	1.1mm ²
[2] CICC 09	150nm/1.55V	NA	2Mb/s MSK	2.405-2.480GHz	8.525mW	-116dBc/Hz ¹	0.88mm ²
[3] JSSC 10	65nm/1.2V	NA	2Mb/s FSK	2.29-2.92GHz	12mW ²	-132dBc/Hz ¹	0.27mm ²
[4] JSSC 08	130nm/1.4V	-22dBm	1Mb/s FSK	2.24GHz max.	14mW	-122dBc/Hz ¹	0.7mm ²

¹ inferred from phase noise plot

² for best performance setting

largely comprised of synthesized digital logic and the amount of analog circuitry is minimized. An oversampling digital phase quantizer is used to alleviate linearity and calibration problems encountered with multi-bit TDCs. A two-point self-calibrating modulation scheme enables modulation at 2Mb/s, which is much higher than the loop bandwidth. The transmitter output spectrum is free of in-band fractional spurs. The prototype transmitter is implemented in 130nm CMOS and occupies an active area of 0.6mm². The transmitter delivers -2dBm to a 50 Ω load using a compact two-stage PA that requires no output matching. The prototype device consumes 17mW from a 1.2V supply.

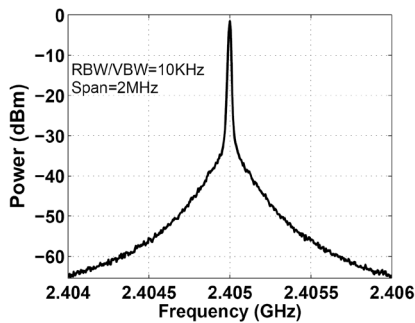


Fig. 6. Measured transmitter spectrum w/o modulation.

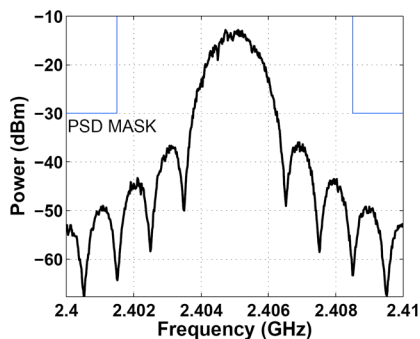


Fig. 7. Measured PLL spectrum w/ 2Mb/s MSK modulation.

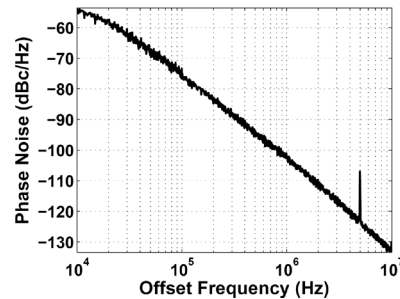


Fig. 8. Measured PLL phase noise at 2.405GHz.

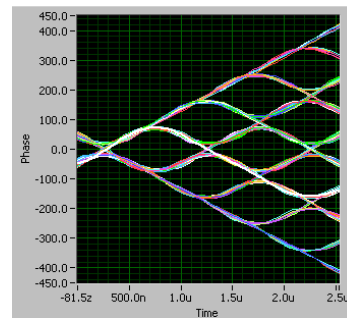


Fig. 9. Measured trellis diagram for 2Mb/s MSK modulation.

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