Rapid Redesign of Analog Standard Cells Using Constrained Optimization Techniques[1]

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ABSTRACT

A first-order analysis of the impact of technology scaling on the performance parameters of linear CMOS analog circuits is presented. Scaling of single gain stage and two-stage operational amplifier small-signal performance parameters is examined under the constant field (CE), quasi-constant voltage (QCV), and constant voltage (CV) scaling rules; in addition to classical full scaling, other practical analog scaling options such as constant device size (W and L), constant total dc bias current, and constant power dissipation are also considered. A computer-aided design tool that accurately and rapidly resizes linear analog standard cells in short-channel CMOS processes using SPICE-quality device models and constrained optimization techniques is described. The CAD tool is applied to redesign a two-stage opamp in 5 μm, 3 μm and 2 μm p-well CMOS technologies for both minimum power dissipation and minimum die area objectives using modified constant voltage (V_{dd} = 5 V) scaling rules. About 10 seconds of computer time on a DEC 3100 are required per optimized redesign.

INTRODUCTION

In 1983, the now classical *digital* scaling laws shown in Table 1 [1]-[2] were applied to determine and predict the impact of technology scaling on the performance of CMOS *analog* circuits [3]. Since that time, it has been assumed that both the analog and digital circuits are *identically* scaled; consequently, the predicted performance of the scaled analog circuitry is severely degraded. In modern mixed-mode integrated circuits, the die area of the analog circuitry typically comprises only about 10-20 percent of the total chip area. In purely practical economic terms, therefore, it is not necessary to scale the analog circuitry in the same way that the digital circuitry is scaled [4]. Hence, it is reasonable to consider several analog scaling options that modify the conventional digital scaling laws such as constant device size, constant total dc bias current, or constant total power dissipation. In many cases, the performance of the scaled analog circuitry in scaled CMOS technologies actually *improves* when the analog scaling options are used as indicated in Table 2. From this key observation, it follows that for a given analog design with a given set of specifications, there exists an *optimum redesign* of the analog cell into a scaled CMOS technology. The purposes of this paper are to demonstrate the use of constrained optimization techniques in the rapid redesign of typical CMOS analog circuits into scaled designs with equivalent performance, and to provide insight into the optimum analog scaling laws.

Scaling Factor = K		
Vertical Dimensions	x	K^{-1}
Lateral Dimensions	W,L	K^{-1}
Voltages	V	K^{-1}
Doping Concentrations	N	K
Junction Cap/area	Cj	$K^{1/2}$
Gate Caps/area	Cox	K

Constant Field (CE).

Scaling Factor = K		
Vertical Dimensions	x	K^{-1}
Lateral Dimensions	W,L	K^{-1}
Voltages	V	$K^{-1/2}$
Doping Concentrations	N	K
Junction Cap/area	Cj	$K^{1/2}$
Gate Caps/area	Cox	K

Quasi-Constant Voltage (QCV).

Scaling Factor = K		
Vertical Dimensions	x	$K^{-1/2}$
Lateral Dimensions	W,L	K^{-1}
Voltages	V	1
Doping Concentrations	N	K
Junction Cap/area	Cj	$K^{1/2}$
Gate Caps/area	Cox	$K^{1/2}$

Constant Voltage (CV).

Table 1. CMOS Technology Scaling Laws.

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	Full Scaling	Constant Size	Constant Current	Constant Power
I	K^{-1}	K^{-1}	1	K
gm	1	1	K	K^2
av	$K^{-1/2}$	$K^{1/2}$	$K^{-1/2}$	$K^{-1/2}$
BW	1	1	K	K^2
BW	K	K^{-1}	K^2	K^3
DR	K^{-1}	K^{-1}	K^{-1}	K^{-1}
DR	$K^{-3/2}$	$K^{-1/2}$	$K^{-3/2}$	$K^{-3/2}$

Constant Field (CE).

	Full Scaling	Constant Size	Constant Power
I	1	1	K
gm	$K^{1/2}$	$K^{1/2}$	$K^{3/2}$
av	$K^{-1/2}$	$K^{1/2}$	$K^{-1/2}$
BW (C fixed)	$K^{1/2}$	$K^{1/2}$	$K^{3/2}$
BW (C scaled)	$K^{3/2}$	$K^{-1/2}$	$K^{5/2}$
DR (C fixed)	$K^{-1/2}$	$K^{-1/2}$	$K^{-1/2}$
DR (C scaled)	K^{-1}	1	K^{-1}

Quasi-Constant Voltage (QCV).

	Full Scaling	Constant Size	Constant Current	Constant Power
I	$K^{1/2}$	$K^{1/2}$	1	K
gm	$K^{1/2}$	$K^{1/2}$	1	K
av	$K^{-1/2}$	$K^{1/2}$	$K^{-1/2}$	$K^{-3/2}$
BW	$K^{1/2}$	$K^{1/2}$	1	K
BW	K^2	1	$K^{3/2}$	$K^{5/2}$
DR	1	1	1	1
DR	$K^{-3/4}$	$K^{1/4}$	$K^{-3/4}$	$K^{-3/4}$

Constant Voltage (CV).

Table 2. Small-signal parameter scaling.

CONSTRAINED OPTIMIZATION

The optimization approach for the rapid redesign of analog standard cells presented in this paper is guided by three principles [5]. First, equations that describe device characteristics are encapsulated and separated from equations that describe the performance of the circuit topologies. Secondly, constrained optimization techniques are used to synthesize the redesigned scaled CMOS circuit. Finally, constrained optimization allows the solution of KCL and KVL constraints to determine the DC operating point, and therefore, only a single DC circuit is solved prior to the optimization process. The nonlinear solver was NPSOL.

The requirements for the design of an analog block are usually formulated in terms of bounds on specified performance parameters such as gain, bandwidth, etc. Analytical expressions are then developed to represent these functions in terms of small-signal model parameters, e.g., $a_v = g_m/g_{ds}$, etc., and subsequently, in terms of design variables W, L, I, etc. These functions can be evaluated by a function call to an encapsulated device evaluator.

An operational amplifier can be formulated as a constrained optimization problem as follows:

$$\min \textit{Area}\ (\mathbf{x})$$

subject to

$$\begin{aligned} \text{Gain } (\mathbf{x}) &\geq \text{GAIN} \\ \text{Slew Rate } (\mathbf{x}) &\geq \text{SLEW RATE} \\ \text{Unity-gain Frequency } (\mathbf{x}) &\geq \text{UGF} \\ \text{Phase Margin } (\mathbf{x}) &\geq \text{PHASE MARGIN} \\ x_L \leq \mathbf{x} &\leq x_U \end{aligned}$$

The variables $\mathbf{x}$ are the bias voltages and currents and device sizes. The function to be minimized (or maximized) is called the objective function and in this example is the die area.

Note that the analytical equations replace the circuit simulations. The equations can potentially be determined using symbolic simulation [6]. The nonlinear solver used was NPSOL [7]. This program used the Sequential Quadratic Programming algorithm to solve constrained nonlinear optimization problems. The constraints are introduced in a multistep manner with the previous solution used as the initial point since nonlinear optimization algorithms are sensitive to initial conditions. The variables are scaled to avoid ill-conditioned gradient matrices.

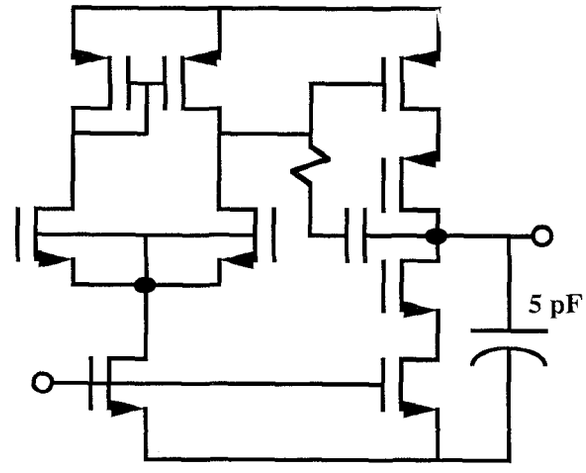

Fig. 1. CMOS two-stage Opamp.

RESULTS

As examples of optimized redesign, the two stage operational amplifier of Fig. 1 was designed in 5, 3, and 2 μm p-well CMOS technologies to meet the design specifications shown in Table 3. Versions with minimum area and minimum power objective functions were considered as shown. Constant voltage scaling was assumed in these examples. SPICE Level 2 models were used to verify the redesigned circuits. The results shown in Table 3 indicate that by allowing variations in bias current or die area, optimum redesigns are obtained that dissipate half as much power or require only about 1/8 as much die area. Typically, 10-20 seconds of computer time on a DEC 3100 was required for each of the optimized redesigns.

Minimum Area Designs				
Parameters	Specs	5 μm	3 μm	2 μm
Gain (dB)	80	101.8	80	80.3
Slew (V/uS)	10	10/14	10/16	10/20
Swing (V)	2.0	2.0	2.0	2.0
UGF (MHz)	5.0	5.0	5.45	5.84
P.M. (Deg)				
Cc (pF)	--	2.26	1.16	1.18
CL (pF)	--	5.46	5.12	5.06
Area (sq um)	--	12712	4425	3383
Power (uW)	--	655	565	677
CPU (sec)	--	18	14	12

Minimum Power Designs				
Parameters	Specs	5 μm	3 μm	2 μm
Gain (dB)	80	108.1	102.1	82.7
Slew (V/uS)	10	10/10	10/10	10/10
Swing (V)	2.0	2.0	2.0	2.0
UGF (MHz)	5.0	5.0	5.02	5.0
P.M. (Deg)				
Cc (pF)	--	1.90	0.82	0.66
CL (pF)	--	5.29	5.38	5.04
Area (sq um)	--	24500	12508	5110
Power (uW)	--	454	351	318
CPU (sec)	--	18	14	12

Table 3. Results of optimized redesigns.

CONCLUSIONS

Practical scaling considerations for CMOS analog integrated circuits have been presented in this paper. In addition to the conventional constant field, quasi-constant voltage, and constant voltage scaling laws applied to digital integrated circuits, analog scaling options including constant area, constant current, and constant power have been developed. Since these options often result in redesigned circuits that exceed the specifications, a nonlinear optimization CAD tool was developed and used to obtain minimum area and minimum power redesigns. The equation-based CAD tool used an encapsulated device evaluator to provide redesigns in about 10-20 seconds of DEC 3100 computer time. The optimum redesigns provide insights into the practical analog scaling requirements.

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