A SAR-Assisted Two-Stage Pipeline ADC

Chun C. Lee, *Member, IEEE*, and Michael P. Flynn, *Senior Member, IEEE*

***Abstract*—Successive approximation register (SAR) ADC architectures are popular for achieving high energy efficiency but they suffer from resolution and speed limitations. On the other hand pipeline ADC architectures can achieve high resolution and speed but have lower energy-efficiency and are more complex. We propose a two-stage pipeline ADC architecture with a large first-stage resolution, enabled with the help of a SAR-based sub-ADC. The prototype 12b 50 MS/s ADC achieves an ENOB of 10.4b at Nyquist, and a figure-of-merit of 52 fJ/conversion-step. The ADC achieves low-power, high-resolution and high-speed operation without calibration. The ADC is fabricated in 65 nm and 90 nm CMOS and occupies a core area of only 0.16 mm^2.**

***Index Terms*—Analog-digital conversion, data conversion, low-power, successive approximation architecture, switched-capacitor circuits.**

I. Introduction

PORTABLE electronic applications, including wireless communication, imaging and video, demand high-resolution ($\geq$12b) and low-distortion analog-to-digital conversion with a signal bandwidth of tens of MHz. The pipeline ADC architecture is popular because it achieves both high resolution and high speed [1]–[3]. However, pipeline ADCs rely on good component matching and require high-gain and high-bandwidth op-amps to achieve good performance [4]. Furthermore, aggressive device scaling in modern CMOS technology, coupled with low supply voltage operation, has made the design of op-amps difficult. Digital calibration schemes [5], [6] and comparator-based op-amp techniques [7], [8] have been proposed to overcome these limitations. Nevertheless, successive approximation register (SAR) converters have surpassed pipeline converters in terms of energy efficiency. Consisting of a comparator, capacitors, switches and control logic, switched-capacitor SAR ADCs have the advantage of minimal analog complexity [9]. The simple analog content makes the SAR architecture well suited to nanometer CMOS processes [10]–[12], but SAR ADCs are limited in speed due to their serial decision making process. Furthermore, the effective resolution of SAR ADCs is limited by comparator noise and limited capacitor matching [10]–[13]. Moderate resolution SAR ADCs suffer from a large input capacitance because large unit capacitors are required to achieve good matching [11], [12].

In this paper, we present the design, analysis, implementation and prototype measurements of a 12b 50 MS/s SAR-assisted two-stage pipeline ADC [14]. Here, for the first time a large MDAC resolution (>4b) is demonstrated in a pipeline ADC. The prototype ADC consists of a 6b MDAC first stage and a 7b SAR ADC second stage. A large MDAC resolution, especially in the first stage of a pipeline, is desired because it helps to achieve lower power consumption and better linearity [1], [3]. However, a challenge in implementing a high resolution MDAC is the high accuracy required for the sub-ADC. Also, a power-hungry active front-end sample-and-hold (S/H) is usually necessary when there is a high-resolution first stage to avoid aperture errors between MDAC sampling and sub-ADC decision.

The architecture presented here uses the SAR technique for the sub-ADC of the first-stage 6b MDAC, which both enables a high stage resolution and eliminates the need for an active front-end S/H. The first-stage MDAC has a "half-gain" implementation, which reduces the required op-amp transconductance required to achieve the same closed-loop op-amp bandwidth. Thus, it reduces the op-amp power consumption. The half-gain MDAC also allows lower op-amp gain for the same differential nonlinearity (DNL). Furthermore, the half-gain MDAC reduces the op-amp output swing which makes it possible to achieve larger op-amp gain. All of these help in eliminating the need for gain calibration. The use of the SAR architecture in the second stage, enables a large 7b resolution in a single stage, eliminating the need for more pipeline stages and reducing power. The stage resolutions (6–7b) are relatively low compared to moderate resolution (9–11b) SAR ADCs [11], [12], which allows the use of large unit capacitors with sufficient matching. In this way capacitor mismatch calibration is not needed in the SAR sub-ADCs of both stages. The prototype 12b 50 MS/s ADC is calibration-free and achieves 64.4 dB signal-to-noise-and-distortion ratio (SNDR) and 75 dB spurious-free dynamic range (SFDR) near Nyquist. The device consumes 3.5 mW from a 1.3 V supply, which is equivalent to a figure-of-merit (FOM) [15] of 52 fJ/conversion-step. The ADC is implemented in a 65 nm CMOS process and occupies a core area of 0.16 mm^2.

Section II analyzes the trade-offs involved in choosing the first stage resolution of a pipeline ADC. Section III describes the prototype ADC architecture in detail and discusses its advantages over conventional pipeline ADC architectures. Finally, Sections IV and V present circuit details and measured results of the prototype ADC, respectively.

Manuscript received August 24, 2010; revised November 28, 2010; accepted December 15, 2010. Date of publication February 17, 2011; date of current version March 25, 2011. This paper was approved by Guest Editor Ajith Amerasekera.

C. C. Lee is with Intel Corporation, Hillsboro, OR 97124 USA (e-mail: leechun2000@gmail.com).

M. P. Flynn is with the Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, MI 48109-2122 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2011.2108133

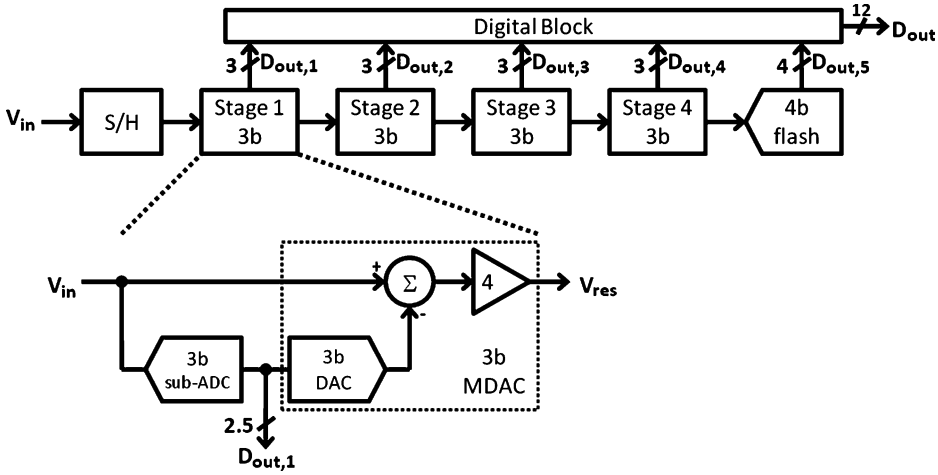


Fig. 1. Conventional 12b pipeline ADC with 3b stage resolution.

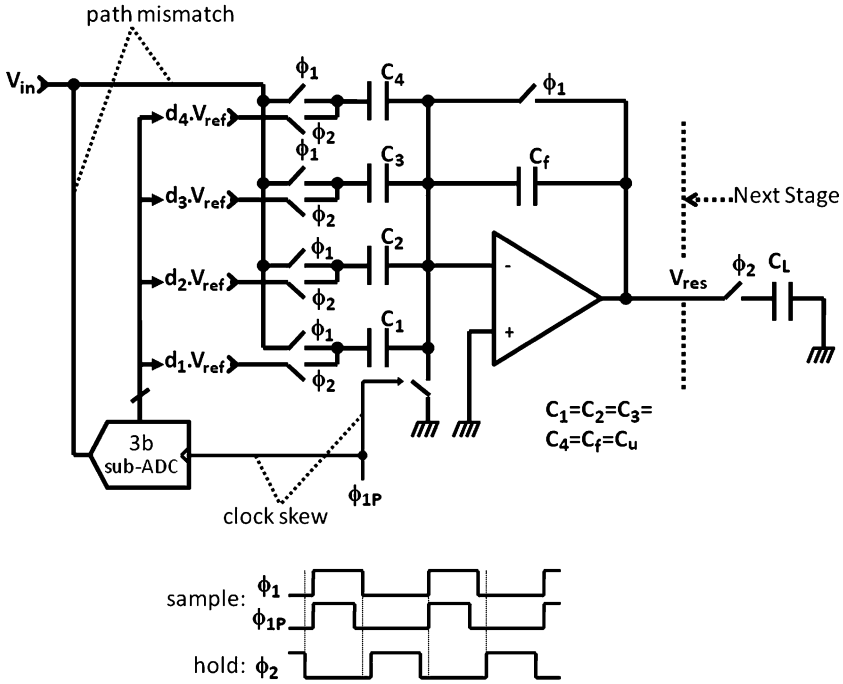


Fig. 2. SC implementation of a 3b MDAC.

II. First Stage Resolution in Pipeline ADCs

A large resolution in the first stage of a pipeline ADC [1], [3] has been shown to be very beneficial for the performance of the ADC as a whole. This is because a large resolution in the first stage reduces power consumption, as well as the noise and nonlinearity contributions of the subsequent stages to the overall ADC performance. However, a large first stage resolution is difficult to implement because of the large number of accurate comparators required to implement a conventional sub-ADC. Furthermore, an active front-end S/H is needed to reduce aperture and sampling errors when a conventional high resolution first stage is employed. This section explains the trade-offs involved in choosing an optimum first stage resolution. Fig. 1 shows a block diagram of a conventional 12b pipeline ADC. As an example, Fig. 2 shows the switched-capacitor circuit implementation of a 3b (2b effective + 1b redundant) pipeline stage, also popularly known as the MDAC stage [16].

A. Power Consumption

The power dissipated in a pipeline ADC is dominated by the front-end stages. This is because the initial stages have the largest accuracy requirement and thus need to dissipate more power in their op-amps to achieve accurate settling. The accuracy required in the subsequent stages decreases exponentially, and thus power dissipated in them is low. It has been shown [1], [3] that a large resolution in the first stage of the pipeline helps decrease the total power consumption of the ADC. We now discuss this in detail.

Assuming a first-order step-response, the output of a first stage MDAC at the end of hold phase ϕ_2 (Fig. 2) can be written as

$$V_{\rm res} = V_{\rm ideal} + V_{\rm err} \quad \text{and} \quad V_{\rm err} = (V_{\rm ideal} - V_{\rm initial}) e^{-\frac{T\beta G_m}{C_{L,\rm tot}}} \quad (1)$$

where T is the time available for settling, β is the feedback factor, G_m is the op-amp transconductance, and $C_{L,\rm tot}$ is the total output load of the op-amp.

For every 1-bit increase in first-stage MDAC resolution M, the feedback factor β ($\approx 2^{1-M}$) decreases by a factor of $\approx$2. This also implies a 1-bit decrease in required resolution of the subsequent stages. Therefore, the poorer feedback factor β is approximately offset by the larger tolerable settling error $V_{\rm err}$. But the output load capacitance $C_{L,\rm tot}$ also decreases approximately two-fold.[1] This allows for the decrease of op-amp transconductance G_m which translates to reduction in op-amp power consumption. The power improvement with the increase in first-stage MDAC resolution ceases after a point. This happens because the output load capacitance $C_{L,\rm tot}$ cannot scale down further when it becomes dominated by the op-amp's output self-parasitics.

B. ADC Linearity

It has been shown [1] that the linearity of a pipeline ADC improves as the first stage resolution increases for two reasons. First, a high first-stage resolution leads to lower nonlinearity from capacitor mismatch. Second, the large gain associated with a high-resolution stage decreases the nonlinearity and noise contributions of the following stages. We now analyze linearity versus resolution in detail.

DNL due to capacitor mismatch[2] in the first-stage of a pipeline ADC has been shown to be [1]

$$\text{DNL} \propto \frac{2^{N-\frac{M}{2}}}{\sqrt{C_{\rm total}}} \quad (2)$$

where N and M are the full ADC resolution and first-stage resolution in bits, respectively. $C_{\rm total}$ is the total input sampling capacitance of the first stage MDAC ($\sum_{i=1}^{4} C_i$ for Fig. 2). We see that ADC nonlinearity, measured in DNL, due to capacitor mismatch, improves by a factor of $\sqrt{2}$ for every 1-bit increase in first-stage resolution. Furthermore, for every 1-bit increase in first-stage resolution, the stage-gain increases by a factor of 2. A larger first-stage gain desensitizes the ADC linearity to the nonlinearities of the following stages.

On the other hand, the ADC nonlinearity due to the finite gain, A, of the first stage op-amp, does not change with stage resolution. Pipeline ADC nonlinearity because of first-stage op-amp gain error, measured as its maximum absolute value of DNL, is proportional to the op-amp gain error $1/A\beta$ and number of quantization steps of the remaining stages 2^{N-M}. It is thus given by

$$|\text{DNL}|_{\max} \propto \frac{2^{N-M}}{A\beta}. \quad (3)$$

For every 1-bit increase in first-stage resolution M, the feedback factor $\beta (\approx 2^{1-M})$ decreases by approximately 2. This is offset by the two-fold increase in the error tolerable at the output of the MDAC, because the total resolution of the remaining stage $(N-M)$ decreases by 1-bit. Thus, nonlinearity, measured as the ADC's $|\text{DNL}|_{\max}$ (in (3)), because of finite op-amp gain A remains the same.

C. Input Sampling Accuracy

During a sampling phase ϕ_1, the input signal $V_{\rm in}$ is sampled onto the array of identical capacitors C_1–C_4 (Fig. 2). During the previous hold phase ϕ_2, the capacitors store DAC reference voltage, $V_{\rm ref}$ or 0 V, depending on the sub-ADC decision in the previous cycle. If the sampling time T is small or the settling time constant[3] τ is large, the previous DAC voltages stored on the capacitors might not be adequately attenuated leading to sampling errors. We show that the performance degradation of the sampling circuit caused by these errors decreases as the resolution of the first-stage MDAC increases.

To explain this effect, Fig. 3 illustrates input signal sampling for the first-stage MDAC. For an input sampling capacitor array of n unit capacitors C_u, assuming the input signal is constant during the sampling period T, and assuming simple *RC* settling, the potential stored on ith capacitor at the end of sampling is given by

$$V_{C,i} = V_{\rm in} + (V_{{\rm prev},i} - V_{\rm in}) e^{-\frac{T}{\tau}}. \quad (4)$$

Here $V_{\rm in}$ is the input signal we want to settle to, and $V_{{\rm prev},i}$ is the prior DAC reference voltage stored on the ith capacitor. $V_{{\rm prev},i}$ depends on the sub-ADC output corresponding to the prior sample and is either $V_{\rm ref}$ or 0 V.

The average of the voltages sampled across all the MDAC capacitors is given by

$$\frac{1}{n}\sum_{i=1}^{n} V_{C,i} = V_{\rm in} + \left(\frac{1}{n}\sum_{i=1}^{n} V_{{\rm prev},i} - V_{\rm in}\right) e^{-\frac{T}{\tau}}. \quad (5)$$

If during the previous hold phase, k unit capacitors are connected to $V_{\rm ref}$ and the remaining $n-k$ capacitors are connected to 0 V, we can write

$$\frac{1}{n}\sum_{i=1}^{n} V_{{\rm prev},i} = \frac{k}{n} V_{\rm ref} = \tilde{V}_{\rm in,prev} = V_{\rm in,prev} + \varepsilon_{\rm prev}. \quad (6)$$

Here $\tilde{V}_{\rm in,prev}$ is the quantized value of the previous input signal sample $V_{\rm in,prev}$ and $\varepsilon_{\rm prev}$ is the associated quantization error.

[1]For the same thermal noise and matching, for every 1-bit increase in first stage resolution, the following stage input capacitance can be decreased by a factor of 4. The minimum unit capacitor size requirements and presence of self-parasitics at the op-amp output limit the total load capacitance scaling to approximately two.

[2]This is assuming that capacitor mismatch error goes as $\Delta C/C \propto C^{-0.5}$; and a unary weighted input capacitor array (C_{1-4} in Fig. 2) implementation.

[3]τ is the product of capacitance C and (source and sampling switch) resistance R.

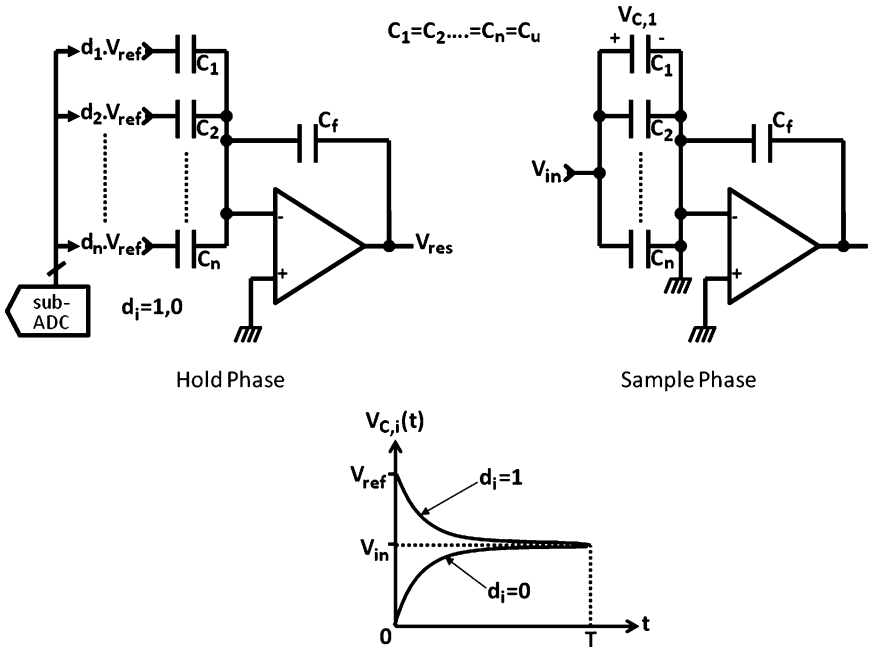


Fig. 3. Input signal sampling in first-stage MDAC.

TABLE I
SAMPLING CIRCUIT RESOLUTION (IN BITS) FOR DIFFERENT VALUES OF FIRST-STAGE MDAC RESOLUTIONS AND AVAILABLE SETTLING TIMES (T/τ)

T/τ	First-Stage MDAC Resolution				
	2b	**3b**	**4b**	**5b**	**6b**
6	10.81	11.75	12.72	13.69	14.67
7	12.26	13.20	14.17	15.14	16.12
8	13.70	14.65	15.61	16.59	17.57

Rewriting (5) we get

$$\frac{1}{n}\sum_{i=1}^{n} V_{C,i} = V_{\text{in}}\left(1-e^{-\frac{T}{\tau}}\right)+V_{\text{in.prev}}e^{-\frac{T}{\tau}}+\varepsilon_{\text{prev}}e^{-\frac{T}{\tau}}. \quad (7)$$

In (7), $V_{\text{in,prev}}e^{-(T/\tau)}$ is a linear function of the previous sample voltage and causes some low-pass filtering, but no noise degradation. On the other hand, $\varepsilon_{\text{prev}}e^{-(T/\tau)}$ is a function of previous sample's quantization error, which is noise, and thus causes SNR degradation. Noise degradation can be large for a small settling time (T/τ) and a small first-stage resolution because of the error $\varepsilon_{\text{prev}}$ being large.

This noise can be removed by shorting out the sampling capacitors at the start of the sampling phase [3]. However, this reduces the effective sampling time T which might not be possible if available sampling time is small. This problem is nearly absent in pipeline ADCs with a large first-stage resolution because quantization error $\varepsilon_{\text{prev}}$ is small.

Table I gives the sampling circuit accuracy (in bits) for different values of settling times (T/τ) and first-stage MDAC resolutions. We see that for a given T/τ, the sampling circuit performance improves by approximately 1b (or 6 dB) for every 1b increase in the first-stage MDAC resolution.

The sampling inaccuracy discussed in this section pertains to non flip-around MDAC architectures with 1b redundancy. As explained in [17], flip-around MDAC architectures with 0.5b redundancy [16] do not suffer from memory-based input sampling inaccuracy. However, non-flip-around MDAC architecture with 1b redundancy is chosen for this prototype ADC because it has a lower output swing requirement[4] for the op-amp, making it more suitable for implementation in low voltage scaled CMOS processes.

D. Sub-ADC Implementation

We now consider the implementation complexity of the sub-ADC with respect to the stage resolution. The sub-ADC of

[4]For example, the sub-ADC comparators at $\pm 3V_{\text{ref}}/4$ thresholds in a 2b non-flip-around MDAC are removed to form a 1.5b flip around MDAC [16]. This causes the 1.5b MDAC output residue $|V_{\text{res}}|$ to be $> V_{\text{ref}}/2$ for $|V_{\text{in}}| > 3V_{\text{ref}}/4$. With no comparator offsets in its sub-ADC, a 2b MDAC output residue $|V_{\text{res}}|$ will be $< V_{\text{ref}}/2$.

a pipeline stage quantizes the input signal and sets the bottom plate switches of the input sampling capacitor array to the appropriate reference voltage for MDAC operation. The sub-ADC is usually implemented as a low-resolution flash ADC and can be of low accuracy due to the presence of redundancy [18]. 2^M comparators are required to implement an M-bit sub-ADC. As M increases, the number of comparators required increases exponentially. Redundancy in the conventional pipeline ADC architecture allows large comparator offsets provided that the sub-ADC output is monotonic.[5] This translates to a maximum comparator offset of $\pm$1/2LSB, where LSB is resolution of the sub-ADC. As the stage resolution increases, the LSB size decreases exponentially, hence the tolerable comparator offset decreases exponentially. Thus, the number of comparators and their accuracy required increases exponentially as the pipeline stage resolution increases, making it difficult to implement large stage resolutions.

E. Phase Mismatch and Clock Skew Errors

Without an active front-end sample-and-hold, the first-stage sub-ADC output might not correctly quantize the input signal stored on the input sampling capacitor array because of phase mismatch and clock skew [19]. The input sampling capacitor array and the sub-ADC (Fig. 2) have different input sampling paths and it is difficult to match the phase delay of these two paths precisely. Moreover, if the sub-ADC is located far from the capacitor array, the sampling clock and the sub-ADC decision clock might be skewed (Fig. 2) causing an aperture error. This leads to decision errors by the sub-ADC, which can be large especially for a high-frequency input signal. Redundancy helps the ADC tolerate decision errors up to $\pm$1/2LSB,[6] but as the first-stage resolution increases, the tolerable error decreases exponentially.

Calibration has been proposed [20] to mitigate these sampling errors, but most calibration methods calibrate out errors for a particular input signal frequency and are thus less effective for other frequencies. Another known method to remove this error is to use an active S/H at the input of the pipeline ADC. An active front-end S/H presents a clean sampled-and-held signal to the input of the first-stage and greatly reduces the effect of phase mismatch and clock skew. But an active front-end S/H adds noise and consumes considerable power. Therefore, these methods are not popular, especially in low-power ADC designs.

III. Proposed ADC Architecture

The architecture[7] we propose in this paper avails of the advantages of a high-resolution front-end stage and eliminates the need for several accurate comparators in the sub-ADC and the need for an active front-end S/H. Fig. 4 shows a block diagram of the proposed ADC architecture. The ADC is a pipeline

[5]This is assuming that the following stage has a sufficient input signal range to accommodate and correct such errors.

[6]This is assuming that the comparators are perfect and have no offsets. Budgeting part of the redundancy to comparator offset further reduces the tolerable phase mismatch and sampling-skew errors.

[7]A similar SAR sub-ADC architecture was independently developed and presented in [21] and [22].

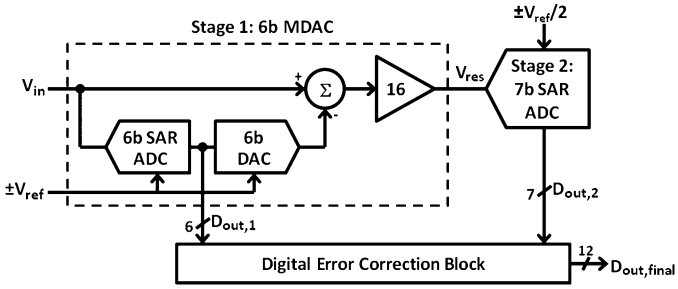


Fig. 4. Proposed ADC architecture.

of 6b MDAC and a 7b SAR ADC. The first-stage MDAC has a 5b effective resolution with 1b redundancy. The first-stage sub-ADC utilizes the MDAC input sampling capacitor array as a CDAC to implement a SAR sub-ADC. This SAR sub-ADC architecture eliminates the disadvantages while retaining the advantages of a high-resolution front-end pipeline stage. The first-stage MDAC has a gain of 16 instead of the usual gain of 32 for a 6b MDAC; we name this as a "half-gain" implementation. The half-gain MDAC reduces the op-amp power consumption and significantly reduces ADC nonlinearity due to finite op-amp gain. The second stage also employs a SAR architecture to efficiently implement a large 7b stage resolution eliminating the need for more pipeline stages. The second-stage also has a "half-reference" implementation which compensates for the first-stage half-gain implementation, without requiring an additional set of half-reference voltages ($\pm V_{\rm ref}/2$). This section analyzes these advantages in detail.

A. SAR Sub-ADC Architecture

Fig. 5 shows the circuit implementation of the 6b first-stage of the pipeline. The flash sub-ADC of a conventional pipeline ADC (Fig. 1) is replaced by a SAR sub-ADC. The MDAC input sampling capacitor array is also utilized by the SAR sub-ADC as its CDAC. The SAR sub-ADC is integrated into the MDAC by connecting a single comparator to the top plate of the input capacitor array. This comparator makes serial decisions and quantizes the signal stored on the capacitor array to 6b, reducing the required number of comparators from 64 to 1.

The problem of sampling path mismatch, described in Section II-E, is eliminated because the SAR sub-ADC and MDAC share the same sampling path, as compared to two different paths in a flash sub-ADC based MDAC. The single comparator quantizes the static signal stored on the capacitor array, hence aperture error is also absent. Thus, this architecture eliminates the need for an active front-end S/H. The MDAC has a large 6b resolution, which greatly reduces the noise part of the sampling error ($\varepsilon_{\rm prev}$ in (7)) discussed in Section II-C. This reduces the performance degradation of the sampling circuit.

A disadvantage of a SAR sub-ADC is the increase in the decision time required for the single comparator to quantize the input signal to 6b. This increased decision time can reduce the available sampling time or the hold time of the MDAC. In our prototype implementation, the MDAC's sampling time is reduced to accommodate the increased decision time. A decrease

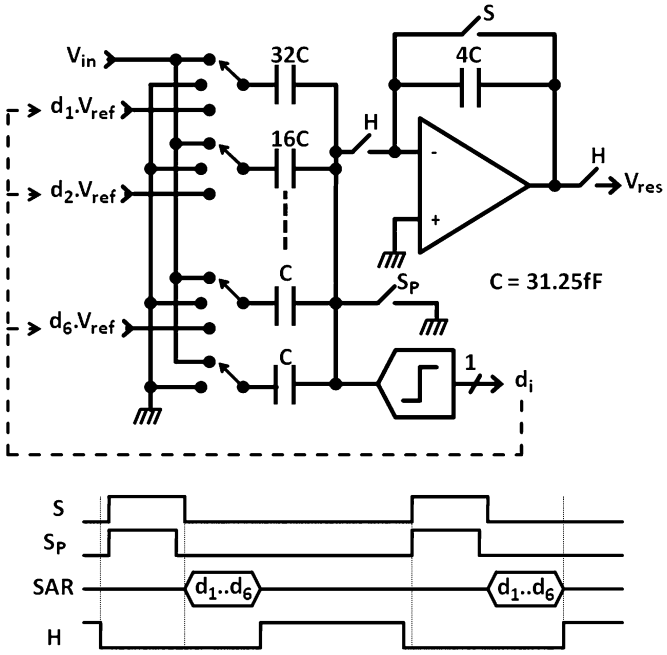


Fig. 5. First-stage 6b half-gain MDAC implementation.

in hold time of the MDAC is avoided as it would have necessitated a larger op-amp bandwidth, and larger power consumption. The disadvantage is further mitigated by using a fast comparator, which requires only 2.4 ns to make 6-bit decisions. This comparator is discussed in detail in Section IV-C.

B. Half-Gain MDAC

The operation of the MDAC is at the point where the output load capacitance $C_{L,\mathrm{tot}}$ (in (1)) is dominated by the op-amp's self-parasitics. Thus, the large first-stage 6b resolution helps achieve the maximum possible reduction in power, as discussed in Section II-A. To further reduce power consumption we propose a "half-gain" MDAC architecture. In this implementation the MDAC gain of 32 (i.e., 2^{6-1}) found in conventional architectures is reduced to 16. This half-gain MDAC helps to further reduce the op-amp power consumption and significantly improves the ADC linearity. We will now discuss these advantages in detail.

The half-gain MDAC implementation helps reduce op-amp power dissipation because it increases the feedback factor β (in (1)) from 1/33 to 1/17. Thus, the closed-loop bandwidth $\beta G_m/C_{L,\mathrm{tot}}$ is increased approximately two-fold. Equivalently, for the same settling error $V_{\mathrm{err}}/(V_{\mathrm{ideal}} - V_{\mathrm{initial}})$ the op-amp transconductance G_m can be decreased by a factor of two.

The half gain implementation also significantly improves the ADC linearity. This is because of two reasons. First, the almost-two-fold increase in β also halves the ADC's $|\mathrm{DNL}|_{\max}$ due to finite op-amp gain-error (in (3)). Second, since the voltage swing at the output of the op-amp V_{res} is decreased by a factor of two, it allows us to stack more cascode transistors in the op-amp (Section IV-B) to enhance the op-amp gain A (in (3)). This further reduces $|\mathrm{DNL}|_{\max}$ due to first-stage gain-error.

In theory, the decreased voltage swing at the MDAC output because of the half-gain implementation, is a disadvantage for the second stage because of the reduced LSB size of the second stage. However, this is not a significant drawback since 7b SAR ADCs are usually not thermal-noise-limited and are easy to implement even in this reduced signal range without any significant increase in the output load capacitance $C_{L,\mathrm{tot}}$. Although a further reduction in the first-stage gain, e.g., a quarter-gain implementation, would be even more advantageous for the first-stage MDAC, this would lead to a greatly reduced second-stage LSB size resulting in a thermal-noise-limited design. For this reason, a larger gain reduction of first-stage MDAC was not implemented to avoid the higher second-stage complexity.

The advantages of the first-stage half-gain MDAC greatly outweigh any disadvantages to the second-stage implementation. These advantages do not apply to the use of a half-gain in low resolution first-stage MDACs (e.g., 1.5b or 2.5b) because decreasing the 1.5b (2.5b) MDAC gain from 2 (4) to 1 (2) would lead to a larger noise contribution from the later stages. Moreover, implementing an 11b or 10b ADC is certainly more difficult than implementing a 7b ADC with the same reduced signal swing.

C. Second Stage Half-Reference SAR Implementation

The second-stage quantizes the first-stage output V_{res} to 7b, within $\pm V_{\mathrm{ref}}/2$. A relatively long half-clock time-period of 10 ns is available for quantization in this stage. Therefore, SAR architecture is chosen to implement this large resolution in a single stage while achieving low power consumption. Fig. 6 shows the implementation of the 7b SAR ADC. As explained in Section III-B, this ADC needs to quantize its input signal in a smaller signal range of $\pm V_{\mathrm{ref}}/2$. In a conventional SAR ADC implementation, this would require half the reference voltages of the first-stage $(\pm V_{\mathrm{ref}}/2)$. To eliminate the need for these additional half-reference voltages, we employ the "half-reference" implementation for the second stage.

In the half-reference implementation, all capacitors are split into two equal halves. During the sampling phase, the input signal is sampled onto the entire capacitor array as in a conventional SAR ADC. However, during the decision phase, when the bottom plates of the capacitors are being switched to the desired reference voltages, only half of the capacitors are connected to full reference voltage $(\pm V_{\mathrm{ref}})$ while the other half are grounded. In this way we get a half-reference implementation without the actual use of $\pm V_{\mathrm{ref}}/2$ voltages. In this implementation, the number of required unit capacitors doubles. Thus, the 7b SAR ADC has a CDAC complexity similar to an 8b one. Alternatively, a 7b ADC in half-signal range can be implemented as an 8b ADC in full-signal range with half of its codes unused. Therefore, the accuracy requirements of the 7b ADC operating with half signal range are the same as that for an 8b ADC in full signal range, which translates to same CDAC requirements in terms of matching and thermal noise.

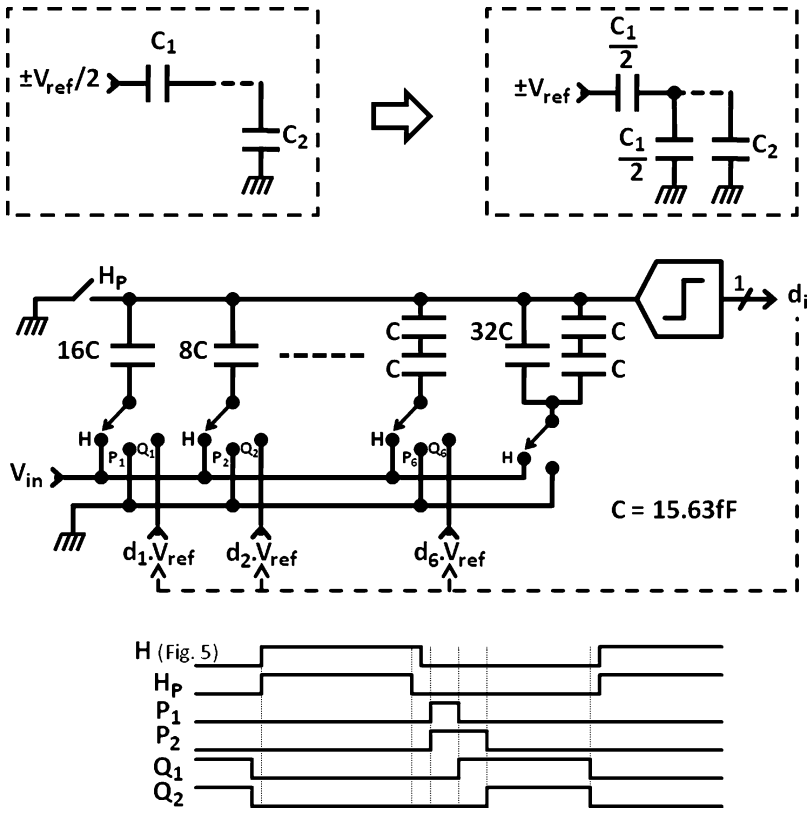


Fig. 6. Second-stage 7b SAR ADC with half-reference architecture.

IV. Circuit Details

A. First-Stage 6b Half-Gain MDAC

Fig. 5 shows the circuit details of the first-stage 6b MDAC. A single-ended version is shown for clarity whereas the actual implementation is fully differential. Most of the architecture details of this stage are explained in Sections III-A and III-B. The array of binary weighted unit capacitors C serves as the input sampling capacitor array for the MDAC as well as the CDAC for the SAR sub-ADC. The single comparator connected to the top plate of the capacitor array is the SAR sub-ADC comparator. This comparator serially quantizes the input signal stored in the capacitor array. There are large voltage excursions on the top plate of the capacitor array during the SAR decision phase. The switch between the top plate of the input capacitor sampling array and the inverting input of the op-amp, controlled by clock phase H, isolates the op-amp from these voltage excursions. This switch introduces a small parasitic capacitance at the input of the op-amp that slightly degrades the feedback factor β of the switch-capacitor circuit. This degradation dictates a slight increase in the gain and bandwidth requirements of the op-amp. The input sampling switches are bootstrapped for better linearity [23]. The sampling time of 7.6 ns, is reduced from 10 ns to accommodate SAR decision phase. This sampling time is sufficient for the sampling circuit to achieve more than 14b precision.

B. First-Stage Op-Amp

Because of 1b redundancy[8] and half-gain MDAC implementation, the first-stage op-amp has a low output single-ended swing requirement of only 250 $\mathrm{mV_{pk\text{-}pk}}$.[9] The low output swing allows the op-amp to be implemented as an nMOS input triple-cascode op-amp (Fig. 7). The tail transistor is biased in the linear region with a $\mathrm{V_{DS}}$ of 70 mV. All other transistors are biased in the subthreshold region with a constant $\mathrm{V_{DS}}$ of 140 mV. With this biasing scheme, the op-amp supports a maximum single-ended output swing of 390 $\mathrm{mV_{pk\text{-}pk}}$ with a 1.3 V supply. Simulations show that this op-amp has a worst case gain of 75 dB across process and temperature variations. A switched capacitor common-mode feedback (CMFB) is used for this op-amp and the feedback correction applied to the tail transistor.

C. First-Stage SAR Sub-ADC Comparator

The SAR sub-ADC comparator needs to be fast so as to have a minimal impact on the sample time available to the MDAC. Dynamic latches [24], often used in low-power SAR ADCs [11], [12], need a large decision time (>200 ps), for two reasons. First, the stack of four transistors between $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$ (M_1–M_4 and M_5–M_7, M_4 in Fig. 8) slows down

[8]1b redundancy halves the output swing of the stage op-amp, provided the sub-ADC is perfect and has no offsets.

[9]To accommodate comparator offsets allowed by redundancy, a larger swing would be required. For a worst case comparator offset an output swing of 500 mV is required.

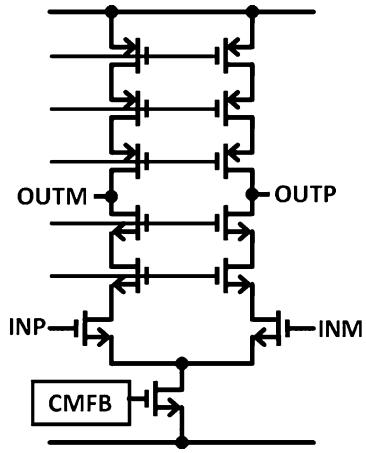


Fig. 7. First-stage op-amp.

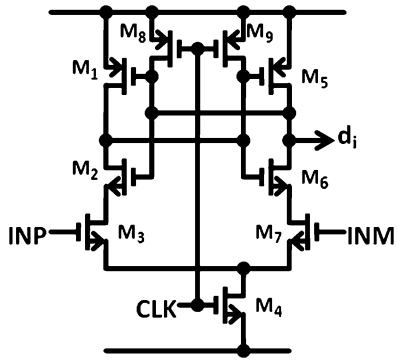


Fig. 8. Dynamic latch [24].

the regenerative process. Second, the gate voltages of the input differential pair (M_3 and M_7 in Fig. 8) are set by the input signal and cannot be biased independently of the input common-mode voltage. This means that we cannot choose a high input common-mode gate voltage for these nMOS devices to force a quick decision. Hence, a dynamic latch is not suitable for this application.

The new comparator introduced here (Fig. 9), is a dynamic preamplifier-based comparator, which has a small decision time ($<$100 ps) and is also low-power. This comparator is a pre-amplifier followed by a latch and operates in two phases, ϕ_1 and ϕ_2. In the ϕ_1 phase, the preamplifier is switched on and it amplifies the input voltage onto the input nodes of the latch. The preamplifier dissipates 1 mA and has a gain of about 2. The pMOS loads of the preamplifier are driven into triode region, therefore the outputs settle very fast with a common-mode voltage near V_{DD}. In the ϕ_2 phase the pre-amplifier is switched off and the latch is enabled. The latch has a conventional design with three transistors stacked between V_{DD} and V_{SS}. Careful sizing of the transistors, coupled with a high initial input voltage, results in a latch decision time of less than 100 ps. The preamplifier is switched on and off dynamically, and ϕ_1 and ϕ_2 are both pulled low when the comparator is inactive, so that the average power consumption of the comparator is very low.

The SAR sub-ADC's CDAC top plate settles during the ϕ_1 phase. The 1b redundancy of the MDAC helps tolerate large sub-ADC decision errors which relaxes the top plate settling

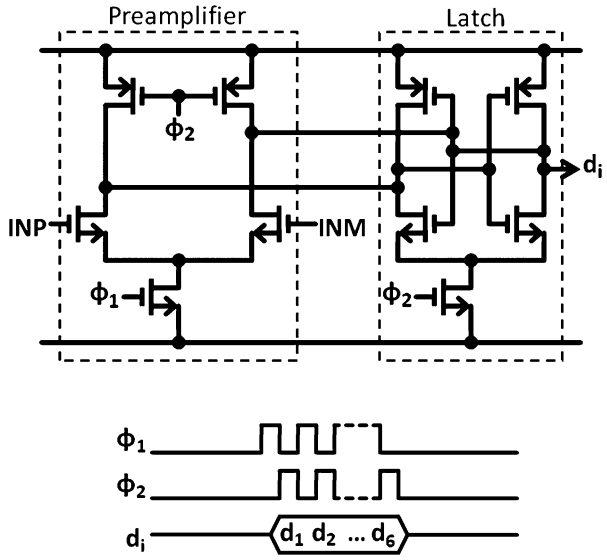


Fig. 9. Dynamic preamplifier-based comparator for first-stage SAR sub-ADC.

requirements for the SAR sub-ADC. Both the ϕ_1 and ϕ_2 phases are each 200 ps long, thus all 6b decisions are achieved in 2.4 ns.

D. First-Stage Clock Generator

An MDAC stage requires non-overlapping clocks to define its sample and hold phases. Non-overlapping clocks are typically generated using an SR latch based circuit [25], shown in Fig. 10(a). The pipeline ADC architecture proposed in this paper requires additional SAR decision clock phases in between the sample and hold clock phases. Fig. 10(b) shows the scheme used to generate all the clock phases required in this new architecture. Delays t_Y inserted in the generation of clock H help generate the multiple delayed clock phases, $\psi_1 - \psi_{13}$. These clock phases are then combined to form the high frequency clock ϕ from which SAR comparator clocks (ϕ_1 and ϕ_2 in Fig. 9) are derived. This clocking scheme generates all the necessary clock phases and also ensures non-overlaps between sample, SAR decision and hold phases.

The end of first-stage sampling, which is the falling edge of clock S_P in Fig. 5, needs to have low jitter to avoid sampling errors. This proposed clock generator ensures a minimal number of inverter delays between the falling edge of external clock CLK and falling edge of S_P. This ensures that little jitter is added to the input signal sampling. Another advantage of this clocking scheme is that the SAR decision clock (ϕ_1 and ϕ_2 in Fig. 9) pulsewidth varies with process and temperature changes tracking the comparator speed.

E. Second-Stage 7b SAR ADC

Fig. 6 shows a single-ended circuit implementation of the second stage 7b SAR ADC. The actual implementation is fully differential. This stage has an implementation similar to that of a conventional SAR ADC. Two unit capacitors C are connected in series to implement a $(1/2)C$ LSB capacitor, reducing the total number of unit capacitors required from 128 to 67. The 32 1/2 unit capacitors, with their bottom plates grounded during SAR search phase, implement the half-reference design, as described

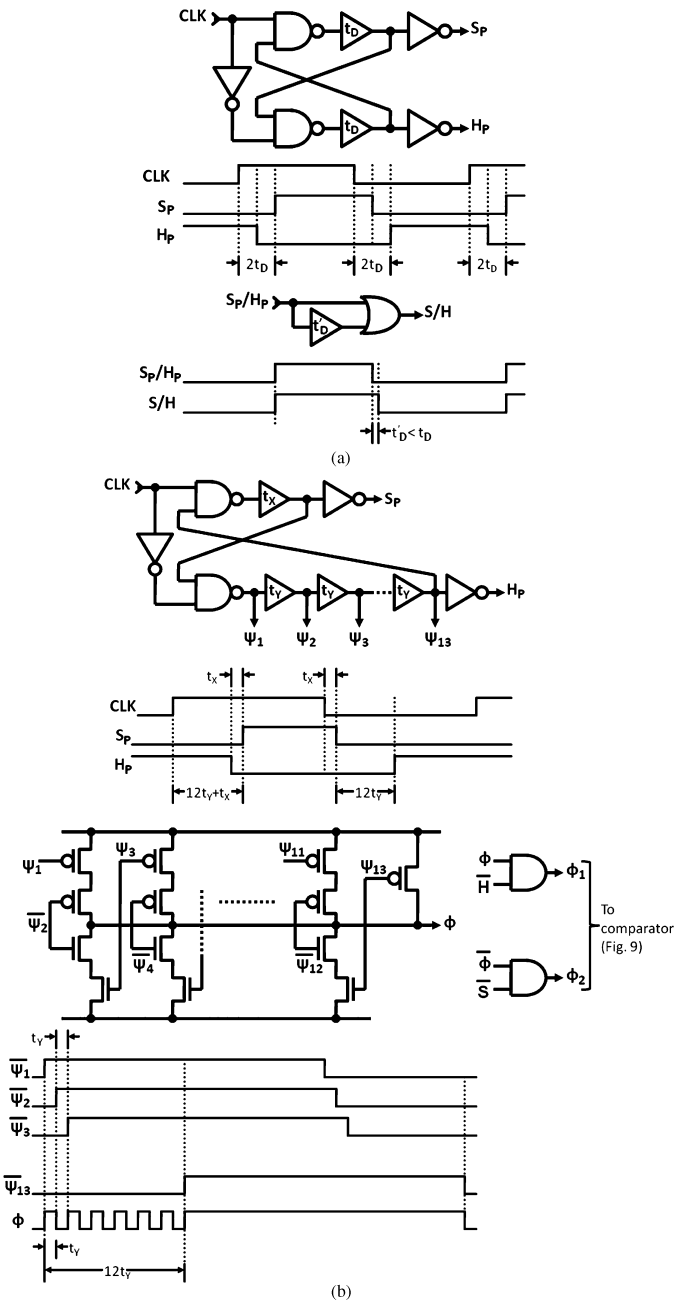


Fig. 10. (a) Conventional non-overlapping clock generator. (b) First-stage clock generator.

in Section III-C. The stage has a sufficient time period of 10 ns to give a 7b decision. Therefore, a low-power, but slower, dynamic latch (Fig. 8) is used as its comparator. Despite the half-gain implementation of first stage, the large front-end gain of 16 almost eliminates the entire noise contribution of the second stage. Thus, capacitor sizing for thermal noise and comparator noise are of little concern in this stage.

The clocks required for this stage are generated using a circuit similar to the one used for the first stage [Fig. 10(b)]. Instead of using the delay generators in a non-overlap clock generator [Fig. 10(a)], a delay-locked loop (DLL) is used to lock the delays for this stage to a half-clock period of 10 ns. This ensures a complete 7b decision within the half-clock period available to this stage.

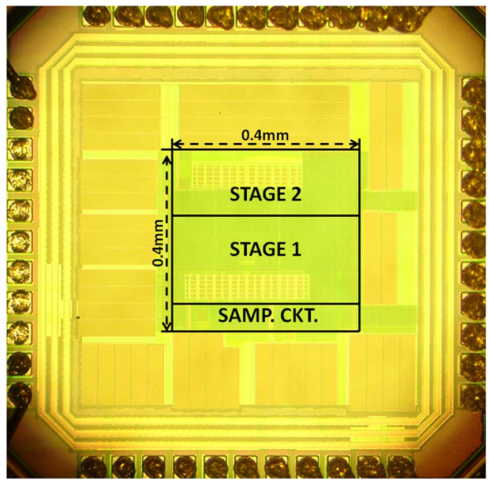


Fig. 11. 65 nm CMOS prototype die microphotograph.

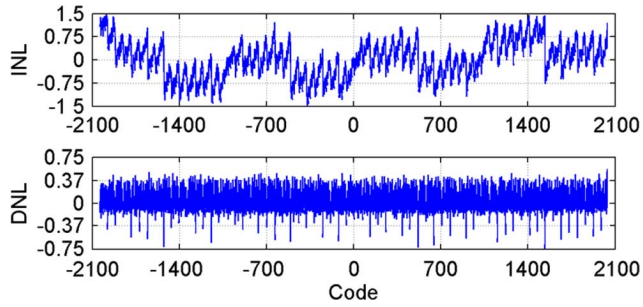


Fig. 12. Measured INL and DNL at 12b level for 65 nm prototype.

V. Measured Results

The prototype ADC is fabricated in one-poly-nine-metal (1P9M) 65 nm and one-poly-seven-metal (1P7M) 90 nm CMOS processes. Very similar measurement results were obtained for the 65 nm and 90 nm prototypes with SNDR differences of less than 0.5 dB. The only difference in design is that the 65 nm prototype does not incorporate the half-reference architecture in its second stage. The core fits within a small footprint of 0.4 mm$\times$0.4 mm, as seen in the 65 nm CMOS die microphotograph (Fig. 11). "SAMP. CKT." in Fig. 11 refers to the input sampling switches and bootstrapping circuit mentioned in Section IV-A. The ADC accepts a full-scale differential input signal of $2\,V_{pk-pk}$ and has a differential input capacitive loading of 1 pF which is small as compared to SAR ADCs of similar or even lower resolutions [11], [12]. Linearity plots (Fig. 12), measured at 12b level for the 65 nm prototype clocked at the full conversion rate of 50 MS/s, show that integral nonlinearity (INL) is within $\pm$1.5LSB and $|\mathrm{DNL}| < 0.75$ LSB. The measured linearity of 90 nm prototype shows INL of within $\pm$1.6LSB and $|\mathrm{DNL}| < 0.8$ LSB. A peak SNDR of 66 dB (10.7b ENOB) is measured for a 2 MHz input signal for the 65 nm design. An 8192 point FFT plot, shown in Fig. 13, demonstrates a 78 dB SFDR for a 4 MHz input signal at -0.5 dB full scale. Fig. 14 summarizes the measured SFDR and SNDR versus input frequency. SFDR and SNDR fall to 75 dB and 64.4 dB respectively for a 20 MHz input signal for both ADCs.

TABLE II
ADC PERFORMANCE SUMMARY

	65nm Design	90nm Design
SNDR (2MHz input)	66dB (10.7b ENOB)	65.6dB (10.6b ENOB)
Conversion Rate (Fs)	50MS/s	50MS/s
Linearity (12b level)	|INL|<1.5LSB |DNL|<0.75LSB	|INL|<1.6LSB |DNL|<0.8LSB
SFDR (4MHz at -0.5dB FS)	78dB	77dB
Input Range	$2V_{pk\text{-}pk}$ differential	$2V_{pk\text{-}pk}$ differential
Input Capacitance	1pF differential	1pF differential
Power Supply	1.3V	1.3V
Power Consumption	3.5mW	3.6mW
FOM [P/(Fs*2^{ENOB})]	52fJ/conversion-step	53fJ/conversion-step
Core Area	$0.16mm^2$	$0.16mm^2$
Process	1P9M 65nm CMOS	1P7M 90nm CMOS

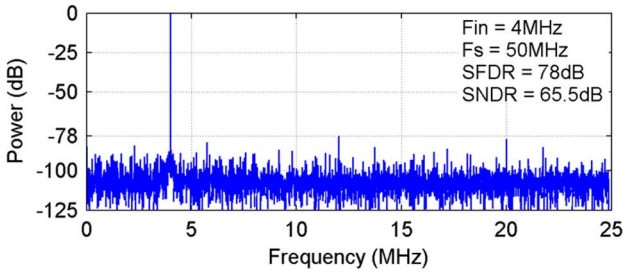


Fig. 13. 8192 point FFT for 4 MHz input (65 nm CMOS design).

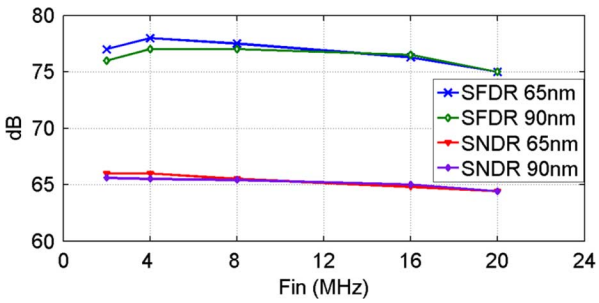


Fig. 14. Measured SFDR and SNDR versus input frequency ($\mathrm{Fs} = 50\,\mathrm{MS/s}$).

The prototype consumes a total power (excluding I/O) of 3.5 mW at the full conversion speed of 50 MS/s. The first stage op-amp consumes 2.6 mW power and the remaining 0.9 mW is consumed by the clock generators and by the first and second stage comparators. The 90 nm ADC consumes slightly larger total power of 3.6 mW. Table II summarizes the measured specifications of the prototype ADCs.

VI. CONCLUSION

This paper proposes a new pipeline ADC architecture, which takes advantage of a large stage resolution in the first stage of the pipeline. This new architecture incorporates a SAR sub-ADC in its first-stage, which eliminates the drawbacks associated with a large resolution pipeline stage. A "half-gain" MDAC is also proposed, which along with the large resolution, helps reduce the power consumption of the first-stage op-amp and improves the ADC linearity. A 7b SAR ADC, implemented as the second-stage of the ADC, eliminates the need for more pipeline stages and further reduces the power consumption.

The prototype ADC demonstrates the ability of this new architecture. The architecture achieves a calibration-free, high-resolution, moderate-speed, area-efficient and power-efficient ADC design, which is difficult to achieve with traditional ADC architectures such as SAR or pipeline. The prototype design consumes only 3.5 mW of power, which translates to a low FOM of 52 fJ/conversion-step.

REFERENCES

[1] W. H. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1931–1936, Dec. 2001.

[2] B. G. Lee, B. M. Min, G. Manganaro, and J. W. Valvano, "A 14-b 100-MS/s pipelined ADC with a merged SHA and first MDAC," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2613–2619, Dec. 2008.

[3] S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath, and P. Wilkins, "A 16b 125 MS/s 385 mW 78.7 dB SNR CMOS pipeline ADC," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 86–87.

[4] S. H. Lewis, "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications," *IEEE Trans. Circuits Syst. II*, vol. 39, no. 8, pp. 516–523, Aug. 1992.

[5] A. N. Karanicolas, H. S. Lee, and K. L. Bacrania, "A 15-b 1-MSample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, Dec. 1993.

[6] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[7] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, Dec. 2006.

[8] L. Brooks and H. S. Lee, "A zero-crossing based 8 b 200 MS/s pipelined ADC," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 460–461.

[9] J. McCreary and P. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques—Part I," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 371–379, Dec. 1975.

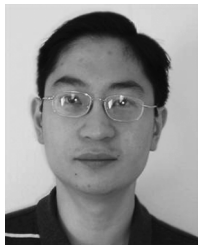
[10] S. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.

[11] J. Craninckx and G. Van der Plas, "A 65 fJ/conv.-step 0-to-50 Ms/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 246–247.

[12] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. Van der Plas, and J. Craninckx, "An 820 μW 9b 40 MS/s noise-tolerant dynamic-SAR ADC in a 90 nm digital CMOS process," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 238–239.

[13] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[14] C. C. Lee and M. P. Flynn, "A 12b 50 MS/s 3.5 mW SAR assisted 2-stage pipeline ADC," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2010, pp. 239–240.
[15] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.
[16] S. H. Lewis, H. S. Fetterman, G. F. Gross, R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-Msample/s analog to digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, Mar. 1992.
[17] J. P. Keane, P. J. Hurst, and S. H. Lewis, "Digital background calibration for memory effects in pipelined analog-to-digital converters," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 3, pp. 511–525, Mar. 2006.
[18] G. G. Gorbatenko, "High-performance parallel-serial analog to digital converter with error correction," in *IEEE National Convention Record*, New York, Mar. 1966.
[19] I. Mehr and L. Singer, "A 55-mW 10-bit 40-Msample/s Nyquist-rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 318–325, Mar. 2000.
[20] H. Jin and E. K. F. Lee, "A digital-background calibration technique for minimizing timing-error effects in time-interleaved ADCs," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 7, pp. 603–613, Jul. 2000.
[21] M. Furuta, M. Nozawa, and T. Itakura, "A 0.06 mm^2 8.9b ENOB 40 MS/s pipelined SAR ADC in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 382–383.
[22] C. P. Hurrell, C. Lyden, D. Laing, D. Hummerston, and M. Vickery, "An 18b 12.5 MHz ADC with 93 dB SNR," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 378–379.
[23] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
[24] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, Apr. 1993.
[25] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. New York: Wiley/IEEE Press, 2004.



Chun C. Lee (S'05–M'10) received the B. Tech. degree in electronics and communication from IIT Roorkee, India, in 2002 and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2006 and 2009, respectively.

From 2002 to 2004, he was a Senior Design Engineer at Texas Instruments, India, where he helped design high-speed analog-to-digital converters. He held a summer internship position at Qualcomm, San Diego, CA, in 2008, where he was involved with the design of low-power high-resolution analog-to-digital converters. He is currently an Analog Engineer with Intel Corporation, Hillsboro, OR. His interests include mixed-signal and RF circuits.

Dr. Lee received the Institute Silver Medal from IIT Roorkee in 2002.

Michael P. Flynn (S'92–M'95–SM'98) received the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, in 1995.

From 1998 to 1991, he was with the National Microelectronics Research Centre, Cork, Ireland. He was with National Semiconductor, Santa Clara, CA, from 1993 to 1995. From 1995 to 1997 he was a Member of Technical Staff with Texas Instruments, DSP R&D Lab, Dallas, TX. From 1997 to 2001, he was with Parthus Technologies, Cork. He joined the University of Michigan, Ann Arbor, in 2001, where he is currently an Associate Professor. He is Thrust Leader responsible for Wireless Interfaces at Michigan's Wireless Integrated Microsystems NSF Engineering Research Center. His technical interests are in RF circuits, data conversion, serial transceivers and biomedical systems.

Dr. Flynn is a 2008 Guggenheim Fellow. He received the 2010 College of Engineering Ted Kennedy Family Team Excellence Award and the 2005–2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan. He received the NSF Early Career Award in 2004. He received the 1992–1993 IEEE Solid-State Circuits Pre-doctoral Fellowship. He is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and serves on the Technical Program Committees of the IEEE International Solid-State Circuits Conference (ISSCC) and the Symposium on VLSI Circuits. He formerly served on the program committee of the Asian Solid-State Circuits Conference, and was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2002 to 2004.