An Integrated 120 Volt AC Mains Voltage Interface in Standard 130 nm CMOS

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***Abstract*—A circuit technique for directly interfacing with 120 V AC mains in conventional CMOS is presented. An on-chip capacitive divider steps-down the 120 V AC supply, which is then regulated. The approach makes use of the very high breakdown voltage of the dielectric between interconnect layers in conventional CMOS technology. This fully integrated scheme is orders of magnitude smaller than traditional approaches. A prototype circuit is fabricated in 130 nm CMOS and converts 120 V AC to a 3.5 V DC supply.**

I. INTRODUCTION

Transformers are used to step-down 120 V AC to voltage levels that can be tolerated on-chip. Discrete transformers and off-chip rectifier circuits constitute a significant amount of board area. Although high voltages can be handled on-chip with specially engineered device structures (e.g. DMOS), these techniques require additional mask levels in a CMOS process [1,2,3]. This work uses a capacitor structure implemented in standard 130 nm CMOS to enable direct interfacing with 120 V AC mains. An on-chip regulator generates a stabilized low-voltage supply. To our knowledge this is the first conventional CMOS integrated circuit that interfaces directly with the 120 V AC line voltage.

This new approach makes tiny, self-contained, mains-powered devices feasible. The elimination of the transformer and of other off-chip elements reduces volume by orders of magnitude. This enables single-chip mains-powered solutions for sensing and telemetry applications. For example chip-scale sensors can be placed throughout a building utilizing the existing mains infrastructure for power. Even μW levels of continuous power are an attractive alternative to batteries or energy-scavenging, and could enable complete sensing and processing nodes.

The circuit topology, the high voltage capacitor design, and the full-wave rectification technique are discussed in Section II. Theoretical analysis of the circuit operation and efficiency are presented in Section III. Measurement procedures and results are given in Section IV.

II. DESIGN DESCRIPTION

The mains interface circuit, shown in Fig. 1, consists of a capacitive divider, a full-wave rectifier, and a voltage regulator. Node V_{AC} is connected directly to the 120 V AC supply. A capacitive divider formed by C_A and C_B steps down the 120 V signal to a level that can be withstood by conventional MOS and metal fringing capacitors. Capacitor C_A is designed to withstand over 200 V, much larger than the breakdown voltages of standard capacitors in the 130 nm process. Diodes D_1 and D_2 rectify the stepped-down voltage signal and charge capacitors C_1 and C_2. The DC voltages V_{DC+} and V_{DC-} are generated on capacitors C_1 and C_2 and power the low dropout regulator (LDO). The LDO uses feedback to ensure that V_{out} tracks V_{ref}. V_{out} is connected to an external load.

Power is transferred from V_{AC} to the load via capacitor displacement current. As V_{AC} experiences a positive cycle the voltage potential at node V_x increases and turns on diode D_1.

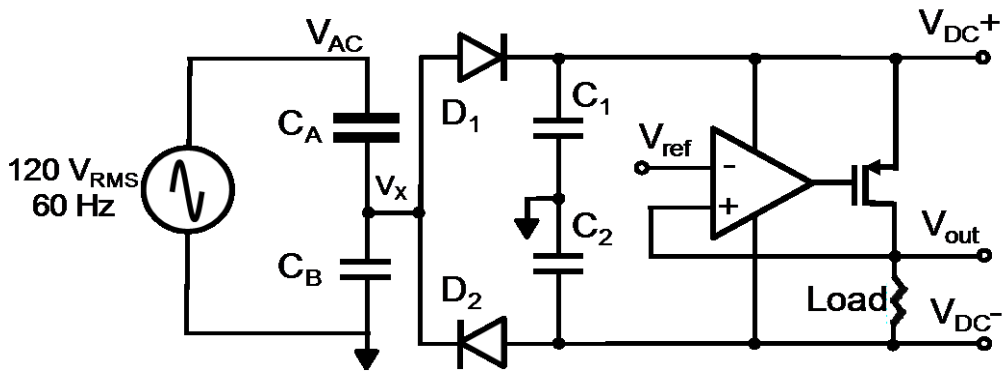

Figure 1. Mains interface circuit schematic

Charge flows from C_A and C_B and accumulates on C_1 until the voltage difference across D_1 becomes zero (assuming an ideal diode model). The displacement current path through C_1 is closed by the connection to ground. The negative cycles of V_{AC} similarly charge capacitor C_2 through diode D_2.

Designing a capacitive transformer circuit at 60 Hz is challenging because the capacitor displacement current is proportional to the slope of the applied voltage signal, resulting in relatively low currents. As an example, a 1 nF capacitor has an impedance of over 2 MΩ at 60 Hz. The large impedance limits the amount of power that can be delivered from the AC source and to a real load.

The front-end of the circuit is a capacitor divider. In the prototype, C_A and C_B are chosen to divide the AC input voltage by 45. This division ratio is chosen to reduce the voltage stress on C_B at the expense of requiring a high voltage capacitor to implement C_A. The peak-to-peak V_{AC} input voltage is

$$2 \cdot \sqrt{2} \cdot 120\text{V} = 339\text{V} \quad . \qquad (1)$$

Assuming voltage division by 45

$$V_x = V_{AC} \frac{C_A}{(C_A + C_B)} = \frac{V_{AC}}{45} . \qquad (2)$$

From (1) and (2) it is calculated that C_A must withstand ±166 V.

A. High Voltage Capacitor

The thick dielectric used to insulate metal interconnect layers in a standard 130 nm CMOS process has a high breakdown electric field which allows construction of high voltage capacitors. A 3D depiction of the capacitor C_A is shown in Fig. 2. The capacitor is composed of the top three thick metal layers in the CMOS process. The capacitor utilizes a fingered metal structure sandwiched between metal layers connected to the *Plus* and *Minus* terminals. Since the breakdown electric field for silicon dioxide is at least 1 MV/cm [4] the metal capacitor plates are separated laterally by 2 µm. The inter-level dielectric thickness is 4µm. The voltage gradient within this structure is below the breakdown electric field, and a reasonable capacitance density of 0.03 fF/µm^2 is achieved. Four banks of 12.5 pF each occupy an area of 0.45 mm^2.

Capacitor C_B needs only to withstand ± 2.8 V, so a custom capacitor design is not necessary. Furthermore, since C_B is much larger than C_A, MOS gate capacitance is used to implement C_B, taking advantage of the higher capacitive density of a FET biased in accumulation. However, since MOS gate capacitors are non-linear, the capacitance varies significantly over the entire range of V_x. Since V_x has both positive and negative cycles, two MOS capacitors are connected in parallel to form C_B. One has its gate node tied to V_x, while the other has its gate node tied to ground. When V_x is positive one device's capacitance increases while the other decreases and vice versa when V_x is negative. Each of the MOS capacitors comprising C_B has a capacitance range from 175 pF to 487 pF over different bias conditions.

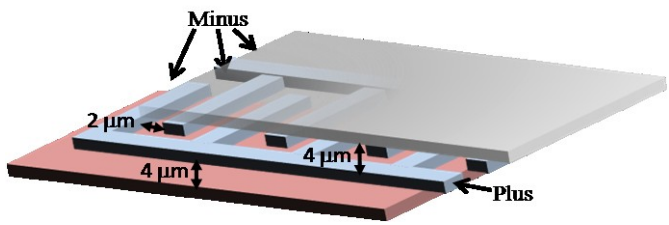

Figure 2. High voltage capacitor structure

Capacitors C_1 and C_2 are each connected in parallel with C_B as D_1 and D_2 turn on and off, affecting the capacitor divider established by C_A and C_B. This extra capacitance decreases the divider ratio by about a factor of 4 and lowers the voltage at V_x. The desired attenuation is achieved by decreasing C_B such that the divider now established by C_A, C_B, and C_1 is 45. C_B cannot be eliminated because it is necessary to ensure V_x does not exceed the breakdown voltage when D_1 and D_2 are both off.

B. Full-wave Rectifier

A full-wave rectifier circuit charges capacitors C_1 and C_2 during the positive and negative AC cycles, respectively. A two-diode center-tapped input full-wave rectifier is shown in Fig. 3(b). It is necessary for C_1 and C_2 to share a common node connected to ground for the charging scheme to operate. This technique center-taps the output and allows full-wave rectification using two diodes instead of four as in the traditional four-diode bridge (Fig. 3a). Since diodes have a non-zero on-voltage, having fewer diodes is advantageous because less power is dissipated in charging C_1 and C_2. Furthermore, without a common node (i.e. if a single capacitor is used instead of the series combination C_1 and C_2) a closed current path for charging C_1 and C_2 does not exist. The voltage difference generated on the series combination of C_1 and C_2 powers the LDO.

3V thick-oxide diode-connected PMOS MOSFETS are used to implement D_1 and D_2. The diode-connected MOSFET is a low-V_{TH} device and turns on when $V_{pos} > V_{neg} + |V_{TH}|$. Two other transistors bias the NWELL of the diode-connected device [5] to ensure the body diodes are always off. These biasing devices operate to connect the bulk to the highest potential (i.e. V_{pos} or V_{neg}).

As the load draws current, charge is depleted from C_1 and C_2. The voltage difference between V_{DC+} and V_{DC-} begins to droop and eventually crosses a threshold where the voltage regulator ceases to operate. During the AC cycle, the capacitor disconnected from V_x, (i.e. either C_1 or C_2) loses voltage as charge is transferred to the load. On the other hand, the capacitor connected to V_x gains charge from the AC source. This property eases the effect of the long time period (1/60 second) between each capacitor reconnecting to V_x on the DC output voltage. Increasing the size of C_1 and C_2 decreases the magnitude of the voltage drop before the charge is refreshed by the rectifier circuit. In this design, C_1 and C_2 are implemented as thick-oxide MOS capacitors, each with a capacitance range of 700 pF to 2 nF.

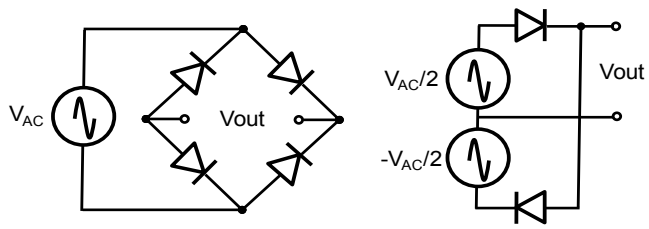

Figure 3. (a) Four-diode rectifier, and (b) Center-tapped rectifier used in prototype

C. *Low drop out regulator (LDO)*

An LDO (Fig. 1) provides a stable output voltage. The LDO is powered by the charge stored on C_1 and C_2. The LDO circuit is composed of thick-oxide MOS devices to withstand the DC output voltage. The amplifier is an NMOS differential pair with a 100 nA tail current with the devices biased in the subthreshold region. A gain and bandwidth of 44 dB and 275 kHz are achieved in simulation. The magnitude of the ripple on the LDO supply voltage, V_{DC+} - V_{DC-}, depends on the size of the storage capacitors and the load. Since the storage capacitors charge and discharge at a low frequency (i.e. 60Hz) the LDO Power Supply Rejection (PSR) of 60 dB prevents the ripple from appearing at the regulated output.

III. ANALYSIS

We consider the circuit in Fig. 1 and assume the capacitors are ideal, lossless components and the diodes are ideal switches. The voltage at V_x is given by

$$V_x(t) = 120\sqrt{2}\sin(2\pi ft)\frac{C_A}{(C_A + C_B + C_1)} \quad (3)$$

where f is frequency (60 Hz) and t is time.

Considering the first half cycle of V_{AC} and ignoring the load current, the circuit is modeled as in Fig. 4. The voltage on C_1, V_{DC+}, is initially 0 V. As soon as V_x becomes greater than 0 V, diode D_1 turns on (the voltage drop across D_1 is zero assuming ideal diode behavior). Diode D_2 is off and capacitor C_2 is disconnected from the circuit. A half cycle of V_{AC} is shown in Fig. 5, where V_{AC} and V_{DC+} are plotted on the left and right axes, respectively. After ¼ period of the input signal the voltages V_{AC} and V_x reach their maximum values.

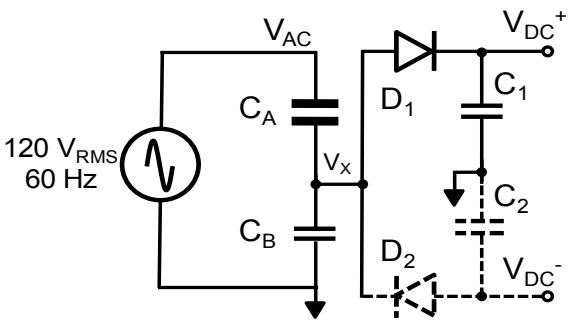

Figure 4. Simplified circuit (dashed section not analyzed)

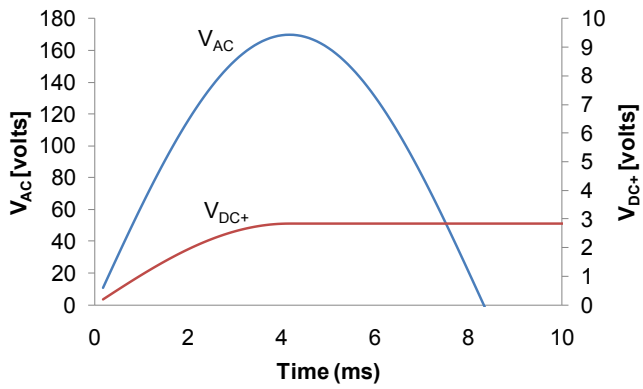

Figure 5. Transient plot of calculated V_{AC} and V_{DC+}

In the following ¼ period V_{AC} and V_x begin to decrease, but since the diode D_1 turns off the voltage on capacitor C_1 remains $V_{x,peak}$.

The average power dissipated to charge capacitor C_1 during the positive cycle is

$$\overline{P} = \frac{1}{T/2}\int_0^{T/2} I_1 V_1 \, dt \quad (4)$$

where T is period (1/60 s), I_1 is the capacitor displacement current, and V_1 is the voltage across the capacitor. The voltage across the capacitor, V_1, between T and T/4 is

$$V_1 = \frac{120\sqrt{2}C_A}{C_A + C_B + C_1}\sin(\omega t) = V_{x,max}\sin(\omega t) \quad (5)$$

where ω is 2π·60 Hz. I_1 is zero between T/4 and T/2. The capacitor current between 0 and T/4 is

$$I_1 = C_1\frac{dV_1}{dt} = V_{x,max}C_1\omega\cos(\omega t). \quad (6)$$

Using (4), (5), and (6) it is shown that

$$\overline{P} = C_1 V_{x,max}^2 f. \quad (7)$$

In this design C_1 and C_2 are 2 nF each and $V_{x,max}$ is approximately 170/45 = 3.77 V. Using (7) the power available from the series combination of C_1 and C_2 is 3.4 μW. The efficiency, η, of the AC/DC converter is defined as the ratio of power delivered from C_1 and C_2 to the power delivered from the AC source.

$$\eta = \frac{P_{deliver}}{\overline{P}} \quad (8)$$

where $P_{deliver}$ is the power dissipated in the load and the LDO. In order to deliver more power to the load $\overline{P}$ must increase. From (7) it is shown that $\overline{P}$ is a function of C_1 and $V_{x,peak}$. The power available from this circuit is a function of C_1 and $V_{x,peak}$, which are limited by on-chip area constraints and maximum on-chip voltages, respectively.

IV. MEASURED PERFORMANCE

The circuit is fabricated in 130 nm CMOS and occupies an active area of 3.5 mm^2. The die photo in Fig. 6 identifies the high voltage capacitor bank C_A and the MOS capacitor arrays that comprise C_B, C_1, and C_2. During testing a high voltage 60 Hz signal is applied to the input while a 3.5 V reference voltage is applied to V_{ref}. A precision current source, connected to $V_{out,}$ acts as a load . Fig. 7 shows the test PCB connected directly to the 120 V AC mains voltage. Fig. 8 shows the transient response of the regulated output voltage when a 120 V AC, 60 Hz signal is applied directly to the chip and V_{ref} is set to 3.5 V DC. A 100 mV ripple (i.e. 2.8 % of supply) is observed on the DC output voltage and is caused by the low frequency rectification. Fig. 9 shows the regulated output voltage as a function of load current when the input reference voltage is 3.5 V and 4 V DC. The measured power delivered to the load is 1.5 µW. Using (8), simulation data for power consumed by LDO, and measured power to the load, an efficiency of 59% is calculated. A summary of prototype IC is in Table I.

The effect of high voltage stress on the capacitor structure is measured by comparing the impedance across C_A before and after a stress test lasting 5 days. The impedance measured across capacitor C_A exceeds 100 GΩ before any voltage stress is applied. After 5 days of continuous operation at 120 VAC the impedance measured across C_A continues to exceed 100 GΩ and the voltage regulator continues to function after the stress test period.

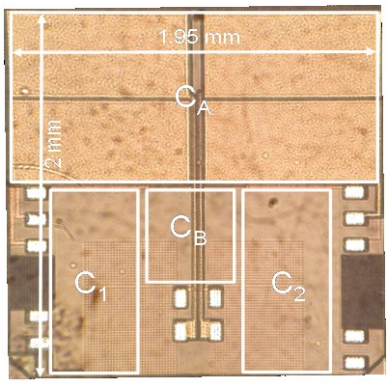

Figure 6. Die photo

Figure 7. Prototype IC connected to 120 V AC mains

TABLE I. SUMMARY OF PROTOTYPE IC

Process	130 nm
Active Area	3.5 mm^2
Input Voltage	120 V AC (mains)
Output Voltage	4 V
Load Power	1.5 uW
η	59%

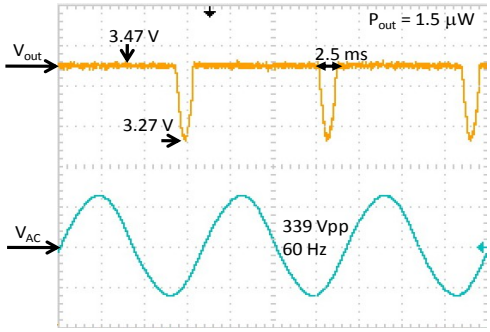

Figure 8. AC input and regulated output voltage

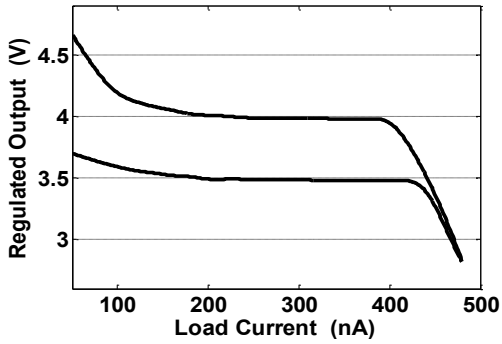

Figure 9. Regulated output vs load. V_{ref} = 3.5V ,4V

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