A Flexible 500MHz to 3.6GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21MS/s SAR ADC

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***Abstract*-A flexible, digital-dominant wireless receiver is implemented in 65nm CMOS. The receive chain consists of a wideband LNA, mixers, and baseband amplifiers. A 7b 21MS/s SAR ADC with embedded, configurable DT FIR/IIR filtering rejects aliasing interferers. Interleaving of sampling and SAR in the ADC maximizes conversion rate. The receiver achieves -92dBm sensitivity, +33dB and +39dB adjacent and alternate channel interferer rejection with 802.15.4 packets, respectively, and -83dBm sensitivity, +41dB, +20MHz interferer rejection with 802.11 packets.**

I. Introduction

The modern day desire for ubiquitous connectivity using multiple standards and bands necessitates the development of flexible, software-configurable receivers. One of the challenges of creating such receivers is the design of low power, configurable filters for rejecting aliasing interferers and adjacent channels. Analog filters become difficult to design at the reduced supply voltages of deep submicron processes. Digital filters require significant over-sampling with a high resolution ADC, at the expense of power consumption, in order to prevent aliasing of the interferer and to capture a weak wanted signal in the presence of a strong interferer.

This work presents a better alternative of embedding a software-configurable, discrete time (DT) filter within a SAR ADC. The DT filter attenuates interference by performing passive charge-sharing, so power consumption and speed improve with process scaling. Compared to receivers with a separate DT filter stage [1,2], the embedded filter reduces capacitor area and saves energy by eliminating charge resampling between the filter and the ADC [3]. Configurability allows the receiver to adapt to its environment and to different communication standards. For example, the receiver can save power by operating in a "no filter" mode when no interferer or adjacent channel activity is present. As the power and the frequency of the interferer change, the receiver can respond by enabling the DT filter and optimally adjusting sampling rate and filter parameters. This 500MHz to 3.6GHz configurable receiver is verified with the 915MHz and 2450MHz bands of the IEEE 802.15.4 standard and the IEEE 802.11 standard.

II. Receiver Architecture

The receiver consists of direct conversion I and Q channels with all the necessary components to receive an RF signal and output digital baseband signals, as shown in Fig. 1. A wideband LNA with matched inputs captures an RF signal and outputs a current signal to a switching mixer. The mixer switches are driven by a 2x LO divider. The down-converted signal is amplified by a chain of baseband amplifiers before filtering and digitization by a 7-bit SAR ADC with embedded, software-configurable DT filtering ("SARfilter ADC").

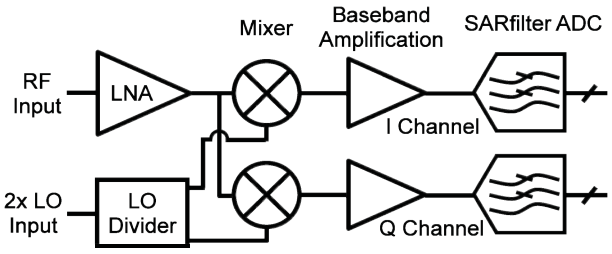

Fig. 1 Block diagram of the SARfilter ADC receiver.

Details of the LNA, mixer, and first stage of the baseband amplifier chain are shown in Fig. 2. The differential LNA [4] achieves low-power and wideband operation by connecting two common-gate and two shunt feedback stages in parallel.

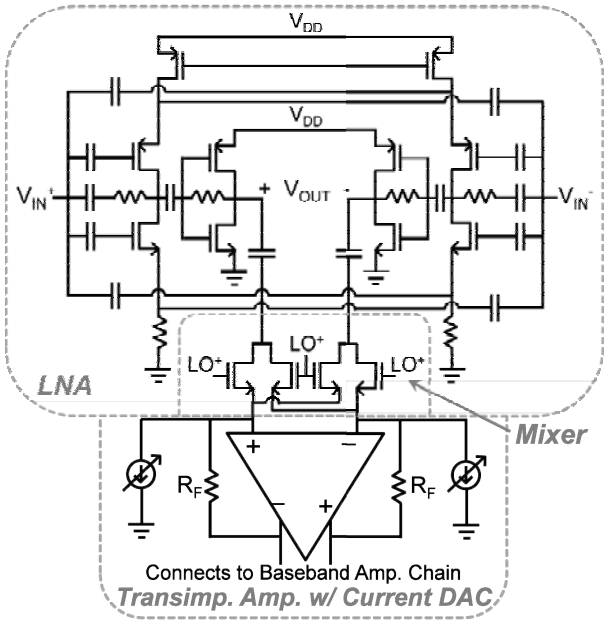

Fig. 2 Simplified diagram of the LNA, mixer, and transimpedance amplifier with binary-weighed current DACs for DC offset correction.

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The parallel combination reduces the total input resistance and power consumption by a factor of 4 compared to an individual common-gate or shunt feedback LNA, at the cost of coupling capacitor area. The output of the LNA is buffered and coupled to passive NMOS mixer switches that drive a transimpedance amplifier. No inductors are used, in order to support a wide range of carrier frequencies, to minimize circuit area, and to maintain compatibility with digital CMOS processes.

A 2x LO divider [5] generates non-overlapping, differential I and Q LO switching signals. Self-mixing of the LO signal and process mismatch can induce a DC offset at baseband. While the use of a 2x LO mitigates the offset error, even a small error can still saturate the baseband amplifiers due to their significant gain. Therefore, binary-weighed current DACs source current from the feedback resistors of the transimpedance amplifier in order to cancel DC offset.

III. SAR ADC WITH EMBEDDED DT FILTER ("SARFILTER ADC")

A. Design of the DT Filter Response

A configurable DT FIR filter replaces conventional baseband filtering. The filter is created by selective sampling of the SAR ADC input onto the unit capacitors of the capacitive DAC, as shown in Fig. 3. The tap weights and delays of the FIR filter are implemented by sampling onto different sized groups of unit capacitors, C_{unit}, over multiple clock cycles [3]. Charge-sharing of the samples immediately before SAR ADC conversion implements the summation that is necessary to create a FIR filtered output.

To create an IIR filter, the collected samples are periodically charge-shared with a history capacitor, C_{IIR}. For example, the filter response described by (1) is created by selectively sampling over 16 clock periods onto groups of $4C_{unit}$ each period. After every 4th sample, the 4 previous samples are charge-shared together and with C_{IIR}, which is sized equal to $32C_{unit}$.

$$y(t) = \frac{1}{48}[x(t-1) + x(t-2) + \cdots + x(t-16)] + \frac{2}{3}y(t-4) \quad (1)$$

B. Interleaved Sampling and SAR Operations

The MSB capacitors of the DAC are duplicated to minimize the reduction of the ADC conversion rate, f_{conv}, caused by selective sampling, which takes as many time units as the number of filter taps. The duplication allows sampling to begin on

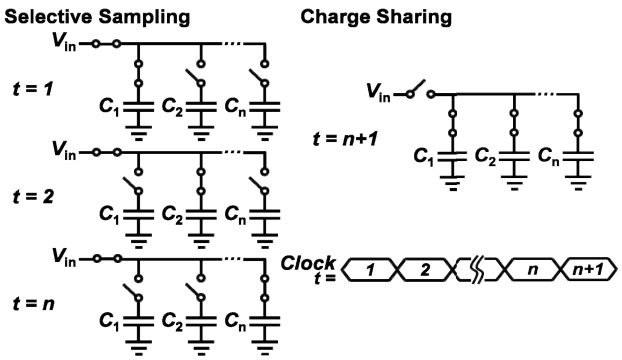

Fig. 3 The DT filter response is created by selectively sampling onto capacitors over multiple cycles, then charge sharing before SAR conversion.

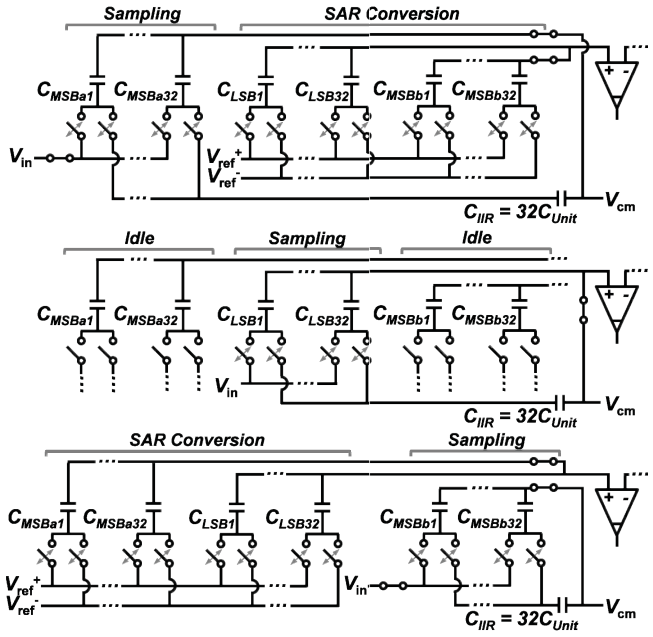

Fig. 4 Interleaved sampling and SAR operations requires the ADC to cycle through: (1) sampling onto MSBa, SAR with MSBb and LSB (top), (2) sampling onto LSB (middle), (3) sampling onto MSBb, SAR with MSBa and LSB (bottom), and (4) sampling onto LSB (middle). Some switches are omitted.

one MSB capacitor bank while the other MSB bank and the LSB bank participate in SAR conversion, as shown in Fig. 4. This improvement in f_{conv} is the key to creating an FIR filter with enough notches to be placed at all of the alias frequencies of a wanted signal that is direct down-converted to DC. These notches reject aliasing interferers before analog-to-digital conversion occurs and prevent the aliases from corrupting the wanted signal. For example, the 16-tap filter shown in Fig. 5 uses interleaving to achieve f_{conv} of 5MS/s with a filter sampling rate, $f_{s,filter}$, of 80MS/s. A 16-tap filter creates 15 notches, which permits placement of an alias suppressing notch at every multiple of f_{conv} between 0 and $f_{s,filter}$. Interleaved operation also facilitates the implementation of IIR filtering, because sampling and charge-sharing with C_{IIR} must occur at a constant frequency, even throughout the SAR conversion process.

C. Implementation Details

The modifications that have been made to the traditional SAR ADC architecture to implement interleaved DT filtering are shown in Fig. 4. The capacitive DAC consists of 96 C_{unit} cells per differential half-circuit. These capacitors are equally

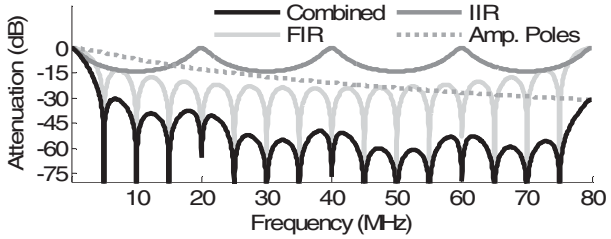

Fig. 5 An example ideal combined filter response and its DT FIR/IIR and amplifier pole components. The DT contribution is described by (1).

divided into MSBa, MSBb, and LSB banks. MSBb is a duplicate of MSBa and permits the implementation of interleaved sampling and SAR operations. Interleaving also requires each of the banks to have dedicated track/hold switches and a switch between the top plates of each MSB bank and the comparator. This switch permits the simultaneous connection of the top plates of one MSB bank to V_{cm} (for sampling) and the top plates of the other MSB bank to the comparator. A switch is added between V_{in} and each C_{unit} to implement selective sampling. An additional switch is added to each C_{unit} cell to create a charge-sharing path between each C_{unit} and C_{IIR}.

D. Ideal Receiver Filter Response

The overall filter response consists of SARfilter ADC DT and baseband amplifier pole components, as shown in Fig. 5. The DT FIR and IIR filter components are described by (1). The FIR filter creates narrowband anti-aliasing notches at multiples of f_{conv} and the IIR filter poles provide wideband attenuation at all frequencies except multiples of $4f_{conv}$. The amplifier poles located at approximately 6MHz and 35MHz provide high frequency attenuation; their locations are determined by amplifier stability design. Together, the filters very effectively reject aliasing interferers and adjacent channels.

IV. Results

The design is implemented in a 1P9M 65nm process with MIM capacitors. The die photo is shown in Fig. 6. The receiver supports RF frequencies ranging from 500MHz to 3.6GHz. Assuming minimal input loss from a matched RF source, which is reasonable given the measured S_{11} of less than -10.5dB, the gain from the RF input to the ADC input is approximately 60dB. The ADC conversion rate can be as high as 21.25MS/s with the 16-tap filter described by (1) enabled, which corresponds to $f_{s,filter}$ of 340MS/s. Power consumption is 3.98mW, 5.51mW, and 9.47mW for 802.15.4 915MHz and 2450MHz bands and 802.11, respectively.

A. Measured Filter Responses

The filter is programmable via a serial interface to operate with 16 to 64 taps and with tap weights from 0 to $6C_{unit}$. Fig. 7 plots the ideal and measured frequency responses by calculating FFTs on the ADC output and measuring the power in the bin corresponding to a down-converted, swept single-tone RF input. The top plot shows the measured response when the 16-tap DT filter described by (1) is configured. The bottom plot shows the measured response when the 20-tap DT filter described by (2) is configured. The "no filter" measurements represent the attenuation provided by the baseband amplifier poles.

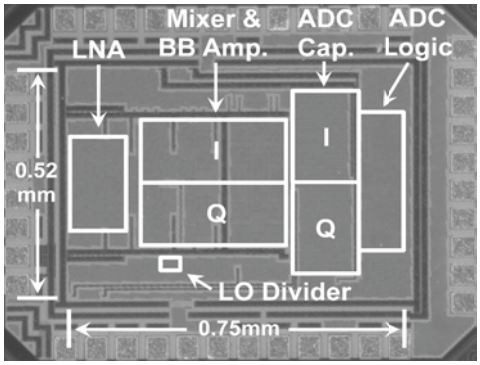

Fig. 6 Die photo.

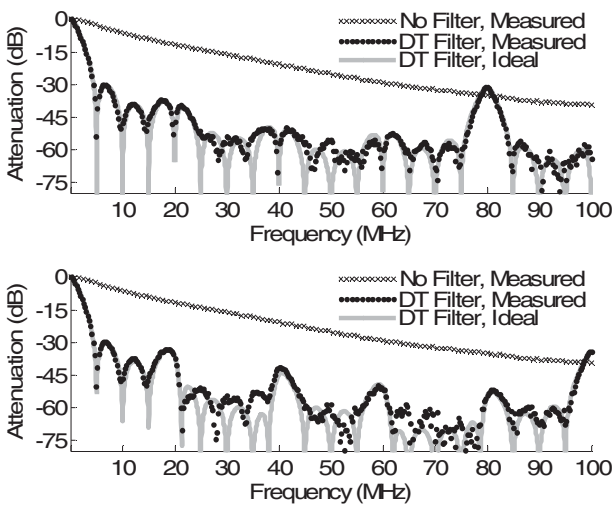

Fig. 7 Measured no filter mode filter response and ideal and measured filter responses for the DT filter described by (1) with $f_{s,filter}$=80MS/s, f_{conv}=5MS/s (top) and by (2) with $f_{s,filter}$=100MS/s and f_{conv}=5MS/s (bottom).

$$y(t) = \frac{1}{192}[3x(t-1) + 3x(t-2) + 4x(t-3) + 3x(t-4) + 3x(t-5) + \cdots + 3x(t-20)] + \frac{2}{3}y(t-4) \quad (2)$$

Although the tap lengths of the two filters differ, f_{conv} is set to 5MS/s in both configurations by choosing $f_{s,filter}$ of 80MS/s and 100MS/s for the 16-tap and 20-tap filters, respectively. The 20-tap filter, with $f_{s,filter}$ of 100MS/s, benefits from a higher pass-band frequency of 100MHz instead of 80MHz, at the cost of power consumption. When combined with amplifier pole attenuation, both configurations attenuate aliasing interferers and adjacent channels above f_{conv} by more than 30dB.

B. Packet Tests

The entire receiver is verified by receiving IEEE 802.15.4 and 802.11 packets. Matched filter demodulation with digital phase correction is performed off-chip. The 802.15.4 tests are performed as required by the IEEE specifications [6], except that only the 20 byte payload is analyzed for bit errors. (Omission of the 6 byte header from error analysis results in <0.2dB error in measured sensitivity.) F_{conv} is set such that the interferer is centered at f_{conv} or $2f_{conv}$, in order to confirm that the DT filter can sufficiently attenuate a worst-case interferer with frequency content that would otherwise alias completely onto the desired signal. The 802.11 tests parameters are chosen to be similar to the IEEE specifications [7]. F_{conv} is set equal to the chip rate and the interferer is set to the channel frequency that is closest to $2f_{conv}$. The desired signal is 802.11 compliant at 1Mbps (11Mchip/s) data rate and framed with a 1024 octet payload. The results of packet testing are plotted in Fig. 8. In 802.15.4 tests, the receiver achieves -99dBm sensitivity and +30dB and +33dB adjacent and alternate channel interferer rejection with 915MHz packets, and -92dBm sensitivity and

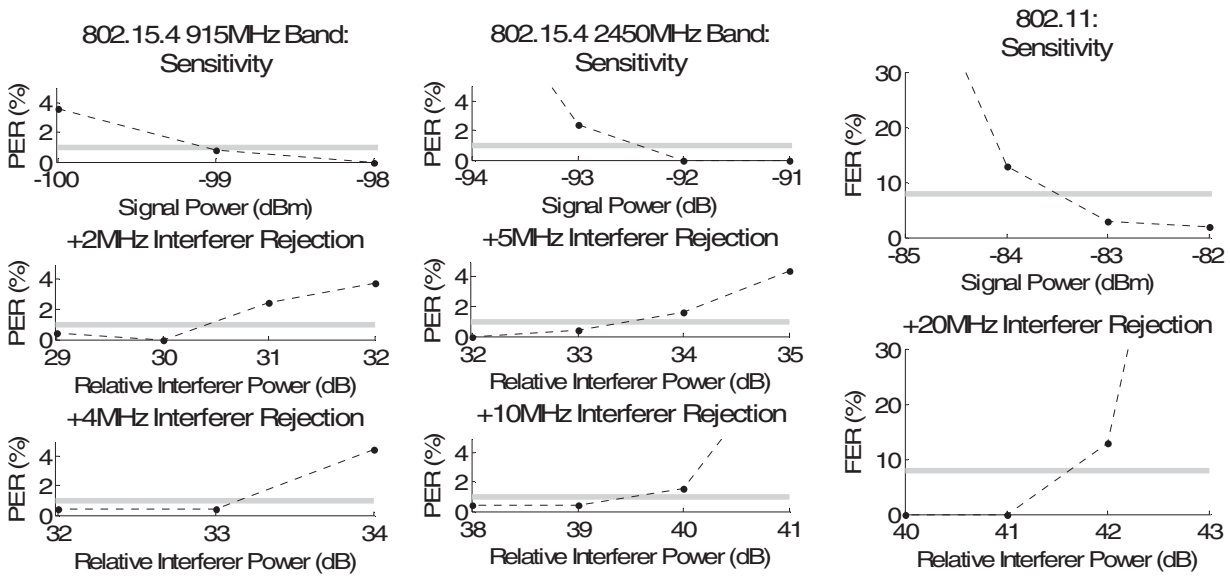

Fig. 8 Packet error rate (PER) and frame error rate (FER) as a function of signal power and interferer power (relative to fixed wanted signal power) for IEEE 802.15.4 915MHz and 2450MHz bands and IEEE 802.11. Each test point represents the error rate calculated from receiving 250 packets. The gray line indicates the maximum PER or FER allowed by the IEEE standards.

+33dB and +39dB adjacent and alternate channel interferer rejection with 2450MHz packets. These results exceed the requirements of the 802.15.4 standard. In 802.11 tests, the receiver achieves -83dBm sensitivity and rejects a +20MHz, +41dB unframed interferer that is 802.11 coded and modulated at 1Mbps (11Mchip/s).

V. Conclusion

A software-configurable DT filter embedded within a SAR-filter ADC enables the creation of a flexible wireless receiver that can adapt to the requirements of a wide range of current and future communication standards and bands.

Acknowledgment

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[7] *Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications,* IEEE Standard 802.11, 2007.

TABLE I
CHIP SUMMARY

Technology		65nm 1P9M w/MIMCAP
Active Area		0.24mm^2
Carrier Frequency Range		500MHz to 3.6GHz
Gain, from LNA to last amplifier stage		≈60dB
S_{11}		< -10.5dB
Noise Figure (simulated)		9dB
IIP3, in-band, from LNA to last amplifier stage		-45dBm
ENOB		≈5b, incl. front-end and baseband amplifier noise and distortion
Maximum f_{conv}, Eq. (1) DT Filter		21.25MS/s
Configurable Filter Tap Length / Weight		16 to 64 / 0 to 6C_{unit}
Power Eq. (1) DT Filter	Analog	5.24mW @ 1.0V 2.79mW @ 0.85V
	Digital	2.16mW @ 1.0V, f_{conv}=11MS/s 0.65mW @ 0.9V, f_{conv}=5MS/s 0.30mW @ 0.9V, f_{conv}=2MS/s
	Clocks, LO Divider	2.07mW, 4.82GHz 2xLO 0.89mW, 1.82GHz 2xLO
	Total	9.47mW, 802.11 5.51mW, 802.15.4 2450MHz 3.98mW, 802.15.4 915MHz
802.11, Eq. (1) DT Filter, f_{conv}=11MS/s Sensitivity and Interferer Rejection		-83dBm; +20MHz, +41dB unframed
802.15.4 2450MHz, Eq. (1) Filter, f_{conv}=5MS/s Sensitivity and Interferer Rejection		-92dBm; +5MHz, +33dB; +10MHz, +39dB
802.15.4 915MHz, Eq. (1) Filter, f_{conv}=2MS/s Sensitivity and Interferer Rejection		-99dBm; +2MHz, +30dB; +4MHz, +33dB