A 12b 50MS/s 3.5mW SAR Assisted 2-Stage Pipeline ADC

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Abstract

A 12b 50MS/s ADC is presented that pipelines a first stage 6b MDAC with a second stage 7b SAR ADC. The first stage uses a low-power SAR architecture for the sub-ADC, to achieve the large 6b stage resolution. A "half-gain" MDAC reduces the output swing and increases the closed-loop bandwidth of the op-amp in the first stage. This ADC consumes 3.5mW from a 1.3V supply, achieves an ENOB of 10.4b at Nyquist, and an FOM of 52fJ/conversion-step.

Introduction

Many electronic applications demand low-power, high-resolution, moderate-speed ADCs. Successive-approximation (SAR) has been the architecture of choice to achieve low-power [1] but its speed and resolution are limited (ENOB $\leq$ 10b) due to capacitor matching, comparator noise and the serial decision making process. Moreover, the large unit capacitors required for good matching result in a large input capacitance. Pipeline ADCs [2] can achieve high speeds but dissipate considerable power in stage op-amps and require complex calibration schemes to achieve accuracy in nanometer CMOS processes.

This paper proposes a novel and power-efficient SAR-assisted pipeline ADC architecture that enables large first-stage MDAC resolution. The prototype ADC pipelines a 6b SAR-based MDAC with a 7b SAR ADC. A large first-stage MDAC resolution in a pipeline ADC improves the overall ADC linearity, power consumption, and relaxes noise and matching requirements [3]. However, in a conventional pipeline ADC it is difficult to implement a large resolution first-stage MDAC because it requires a large number of accurate comparators in the flash sub-ADC and an active front-end S/H [4]. The architecture proposed here uses a SAR, instead of the conventional flash architecture, for the sub-ADC. This eliminates all the drawbacks of a high-resolution MDAC. The first stage also implements a "half-gain" MDAC that reduces the op-amp power consumption and increases its open-loop gain. The use of the SAR architecture for the second stage, helps reduce power and achieve high-resolution, thus eliminating the need for more pipeline stages. The prototype ADC achieves a peak ENOB of 10.7b, no missing codes at 12b resolution and consumes only 3.5mW at 50MS/s.

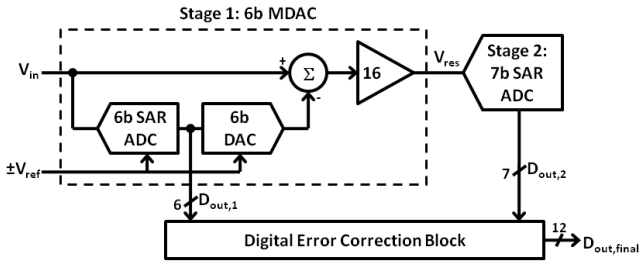

Fig. 1: ADC Architecture

Architecture and Circuit Implementation

Fig. 1 shows the proposed ADC architecture. Fig. 2(a) shows the single-ended circuit implementation of the first stage MDAC and a timing diagram. The actual implementation is differential. The input sampling capacitance of the first-stage MDAC also functions as the capacitive-DAC (CDAC) for its SAR sub-ADC eliminating the need to match the sampling paths of the MDAC and its sub-ADC [4] or to use a dedicated front-end S/H. The single SAR comparator sequentially sets the CDAC reference switches from MSB to LSB. The use of one comparator, compared to 63 in a flash architecture, reduces power consumption in the sub-ADC. A disadvantage of using the SAR architecture is the larger decision time required by the sub-ADC, which reduces either the sample, or the hold time available for the MDAC. In the prototype ADC the sample time is 7.3ns (compared to the half-clock period of 10ns), which is still sufficient for the sampling circuit to achieve >12b resolution. The alternative of decreasing the hold time of the MDAC would require a larger bandwidth from the op-amp. The input sampling switches are boot-strapped for better linearity.

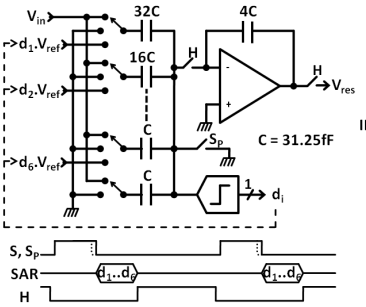

Fig. 2(a): Stage 1 Implementation

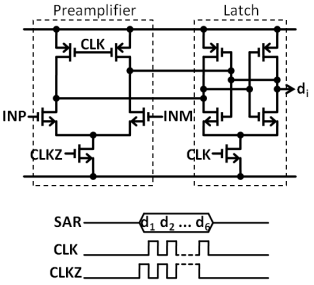

Fig. 2(b): Stage 1 Sub-ADC Comparator

A half-gain MDAC reduces the op-amp power consumption and increases its open-loop gain. For an N bit pipeline ADC with a large M bit front-end MDAC resolution, a high MDAC gain of 2^{M-1} is required. But the output of the MDAC needs to be only (N-M+1) bit accurate. An analysis of front-end MDAC resolution versus required op-amp bandwidth [5] shows that since the larger 2^{M-1} gain requirement is offset by the lower (N-M+1) bit accuracy requirement, the required bandwidth stays the same over different values of M. It is possible to decrease the required op-amp bandwidth (and hence reduce op-amp power dissipation) by breaking this resolution-bandwidth tradeoff. We propose a "half-gain" architecture in which the gain of the 6b MDAC is decreased from 32 to 16. This has two advantages. First, the feedback factor increases from 1/33 to 1/17, increasing the closed-loop bandwidth approximately two-fold. Equivalently, for same settling error, the op-amp bandwidth can be decreased two-fold. Second, the voltage swing at the output of the op-amp decreases, allowing us to stack more cascode

transistors in the op-amp to enhance the op-amp gain. The half-gain first-stage reduces the amplitude of the residue signal passed to the second stage, but the amplitude is still large enough so that the second-stage 7b ADC is not noise limited.

The first-stage MDAC op-amp is implemented as telescopic triple-cascode with an NMOS-input and has a minimum gain of 75dB. The tail transistor is biased near the linear region with a V_{DS} of 70mV and all other transistors are biased in sub-threshold with a constant V_{DS} of 140mV. With this biasing scheme, the op-amp supports a maximum output swing of 390mV with a 1.3V supply. This output swing is more than sufficient due to the reduced swing requirements of the half-gain implementation.

The first-stage SAR sub-ADC comparator (Fig. 2(b)) achieves a smaller decision time (<100ps) compared to the dynamic latch used in [1]. A preamplifier with a gain of 2, dissipates 1mA peak current to attain good settling and reduce input referred offset. This preamplifier is switched on and off dynamically, so the average power consumption of the comparator is low. The first-stage MDAC has 5b effective resolution with 1b redundancy. This 1b redundancy allows for large sub-ADC decision errors, which relaxes the SAR sub-ADC's CDAC top plate settling requirements, and reduces the total decision time. The SAR sub-ADC needs 2.4ns to give a complete 6b decision.

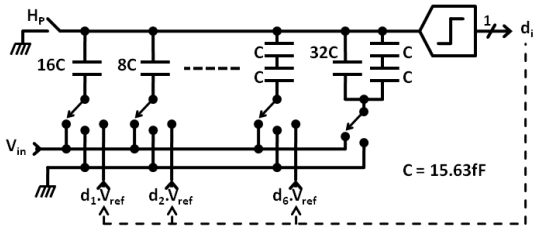

Fig. 3: Stage 2 7b SAR Implementation

Because of the first-stage half-gain MDAC implementation, the second-stage 7b SAR ADC quantizes the residue signal from the first stage with half the overall input signal range. In a conventional SAR architecture this would require half-reference voltages ($\pm V_{ref}/2$). Instead, in the second stage implementation (Fig. 3) the bottom plates of only half of the capacitors are connected to the reference while the remaining are grounded. This explains the presence of 32½ unit capacitors grounded during the SAR search phase. Thus a "half-scaled reference" is implemented without the need for $\pm V_{ref}/2$ reference voltages. In this implementation, the number of unit capacitors required doubles. However, the advantages of the "half-gain" MDAC in first stage far outweigh the disadvantages of increased second stage complexity.

The second-stage SAR ADC has a sufficient half-clock period of 10ns to give a 7b decision. Hence a simpler but slower dynamic latch is used as the comparator for second-stage ADC to reduce power consumption. The large first-stage MDAC gain of 16 almost eliminates the noise contribution of the second stage. Thus the capacitors are sized for matching instead of thermal noise. Comparator noise is also of little concern for this reason.

Measurement Results and Conclusion

The prototype, fabricated in 1P9M 65nm CMOS, occupies a core area of 0.16mm^2. The ADC accepts a full-scale input signal of 2Vpp differential. The input capacitance is only 1pF differential, which is low compared to SAR ADCs with similar or even lower resolutions [1]. Fig. 4 shows the INL and DNL plots, which indicate no missing codes at 12b resolution. A peak SNDR of 66dB (10.7b ENOB) is achieved for a 2MHz input. An 8192 point FFT plot, shown in Fig. 5, demonstrates 78dB SFDR for a 4MHz input signal at -0.5dB full scale. Fig. 6 summarizes the measured SFDR, SNDR versus input frequency. SFDR and SNDR fall to 75dB and 64.4dB respectively for a 20MHz input signal. The chip consumes 3.5mW at the full conversion speed of 50MS/s.

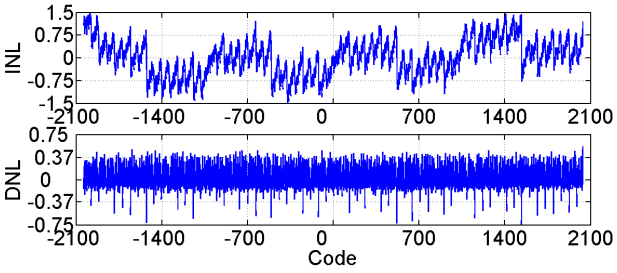

Fig. 4: Measured INL and DNL at 12b level

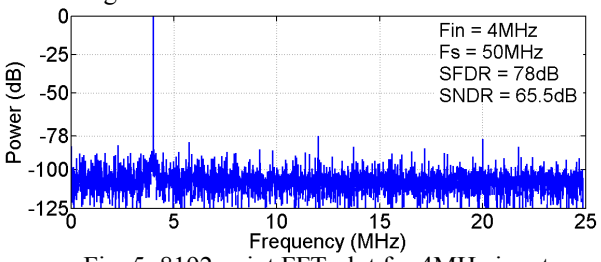

Fig. 5: 8192 point FFT plot for 4MHz input

This paper proposes a new SAR-assisted 2-stage pipeline ADC architecture. The ADC achieves a very low FOM of 52fJ/conversion-step, which is the best reported to date among all ADCs with SNDR > 54dB.

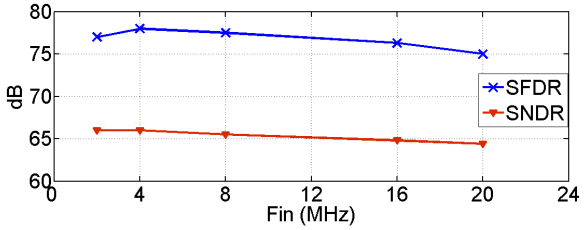

Fig. 6: SFDR & SNDR vs. input frequency (Fs = 50MHz)

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