A High-Performance 1μm CMOS Current Controlled Oscillator[†]

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Abstract

A simple fully symmetrical current controlled relaxation oscillator is presented. The oscillator is based on a novel two capacitor architecture. This fully symmetrical architecture permits relatively large capacitor voltage waveform amplitudes, thus minimising jitter. The use of a fast double differential latching comparator allows high speed operation, with good control linearity. The circuit was successfully fabricated in the 1 micron ADCIS analog CMOS process.

1 Introduction

Controlled oscillators are extremely useful circuits, particularly in telecommunications. Ideally these circuits should be temperature independent, and provide linear frequency control of a low jitter waveform. High control linearity is essential in applications, such as FM demodulation, where nonlinearity contributes distortion to the demodulated signal. However, low jitter operation is more important in clock recovery systems.

It has been shown [1] that noise in relaxation oscillators is minimised by maximizing the amplitude of the timing capacitor voltage waveform. A 5V supply, 3μ CMOS, controlled oscillator with a 5V amplitude capacitor waveform has been described [2]. This circuit used an elaborate technique involving a floating capacitor to generate large capacitor voltage swings. However, because node voltages in excess of the supply voltage are a feature of this circuit, this scheme is unsuitable for small geometry processes, where the supply voltage is often very close to the maximum permissible voltage. More recently a high performance 5V bipolar controlled oscillator has been reported[3].

A simple 5V CMOS oscillator design, suitable for small geometry processes is presented here. A novel twin capacitor architecture permits relatively large voltage swings and is fully symmetrical. All components are on chip.

2 Circuit

A block diagram of the oscillator is shown in figure 1. Two identical capacitors are charged and discharged by identical charge and discharge circuitry. MOSFETs MO2 and MO3 supply

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charging currents equal to the control current IIN. MOSFETs MO4, MO5, MO6 and MO7 control the charge and discharge of the capacitors. The double differential latching comparator, shown functionally as two comparators and a latch, decides when a voltage threshold has been reached. No level shifting circuitry is required.

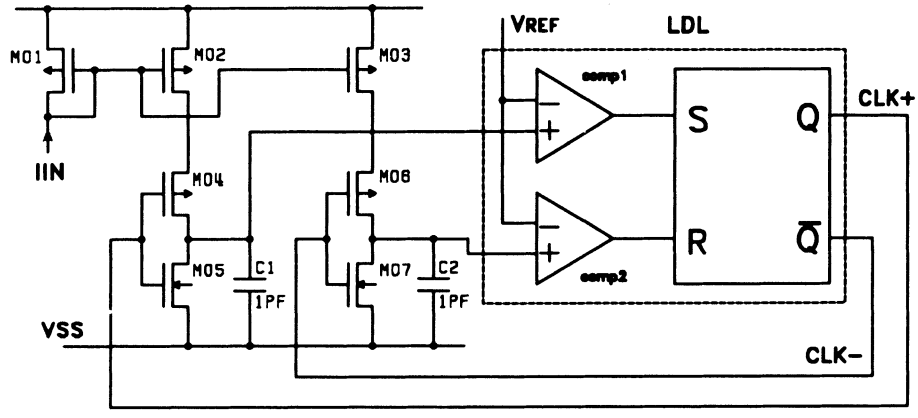

Figure 1: Block diagram of oscillator.

To understand how the oscillator works, assume that initially CLK+ is low, thus allowing a current equal to IIN to charge the capacitor C1. CLK-, the compliment of CLK+, is high. Assume that the capacitor C2 has fully discharged through MOSFET MO7. Charging of C1 will continue until V_{C1} exceeds V_{REF}. Very shortly after this happens comparator 1 switches, changes the state of the latch, causing CLK- to drop low and CLK+ to go high. Capacitor C2 now begins charging through MO6, C1 meanwhile is rapidly discharged through MO5. C2 will continue charging until it reaches V_{REF}, at which point the latch changes state and the entire cycle repeats.

During discharge the timing capacitors are connected directly to VSS by MO5 or MO7. Discharge proceeds rapidly and is completed well before the second (charging) capacitor reaches its threshold. Thus the oscillation period is determined solely by charging cycles, and the oscillation frequency is specified by the control current IIN.

This oscillator structure has many advantages. It is fully symmetrical. As all switchings occur under the same conditions, and capacitor parasitics and nonlinearities affect both capacitors equally, an even duty cycle should be achieved. Additionally, because each waveform has only one comparison point per cycle, relatively large amplitude waveforms (more than 3V) are feasible, thus minimising jitter. The elimination of level shifting circuits, and their associated noise, further reduces output jitter.

2.1 Double Differential Latching comparator

In order to improve oscillator performance, Wakayama and Abidi combined comparison and latching in a double differential latching comparator [2]. A simpler but equally effective variant is described here (figure 2). MOSFETs ML2, ML3, ML6 and ML8 (and MR2, MR3 MR6 and MR8 on the right) resemble the differential pair and active load of a classical CMOS comparator. However, the presence of an additional resistor and transistor in each comparator (transistor ML7 and resistor RL on the left, MR7 and RR on the right), allows the comparator state to be latched on the parasitic capacitances of nodes C and D. Assume initially that node C is low and node D is high. MOSFET ML7 is off and the gate voltage of ML8 is determined by the current flowing through the similar transistor ML6. If now V_{ILM} becomes less than V_{ILO}, then the current flowing through ML3 exceeds that flowing through ML6. Node C rises rapidly,

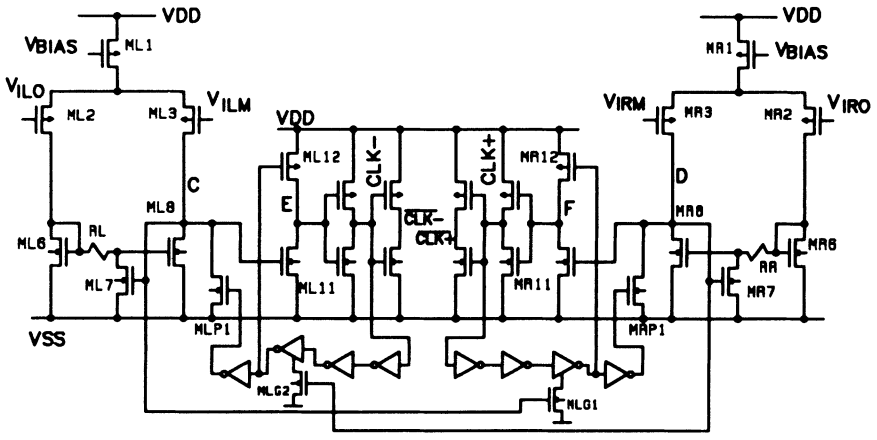

Figure 2: Double differential latching comparator.

turning on ML7, and thus turning off ML8. Meanwhile, the high value of C propagates through the logic circuitry, and turns on the pull down MRP11, for a time determined by the delay inverters, sufficient to fully discharge node D. Also MR12 is turned on for a time sufficient to charge up node F. The latching comparator has now completely changed state. Its state will again change when V_{IRM} becomes less than V_{IRO}.

In order to optimize latching speed the capacitive load on nodes C and D must be small. During switching a minimum sized MOSFET ML11 (and MR11) in the first inverter can quickly discharge node E or F. Similarly MLG1 and MLG2 in the logic circuitry are also small. Complementary buffered signals CLK-bar and CLK+bar are provided by the circuit.

3 Relationship Between Control Current and Frequency

In the ideal case, when there is no switching delay at the threshold points, the oscillation frequency is directly proportional to the control current. The frequency f_0 is related to the control current, and amplitude $(V_{REF} - V_{SS})$, as follows

$$f_0 = \frac{IIN}{2C(V_{REF} - V_{SS})} \tag{1}$$

In reality because of the finite speed of the comparison and switching circuitry, the switchings do not occur exactly when a threshold is reached, and nonlinearity is introduced. If there is a delay of $T_d/2$ between the instant that one capacitor voltage reaches a threshold, and charging begins of the second capacitor, then the actual oscillator frequency f_1 is

$$f_1 = \frac{f_0}{1 + f_0 T_d} \tag{2}$$

The delay time (T_d) is used as a figure of merit for control nonlinearity.

4 Experimental Results

The oscillator was fabricated using the 1μm 5V, double poly, analog CMOS ADCIS process. The circuit is compact, occupying an area of only 50000μm^2. The timing capacitors were implemented using high linearity double poly structures. However, for reasons already discussed, cruder structures (eg poly-n^+) can be used without detrimental effects.

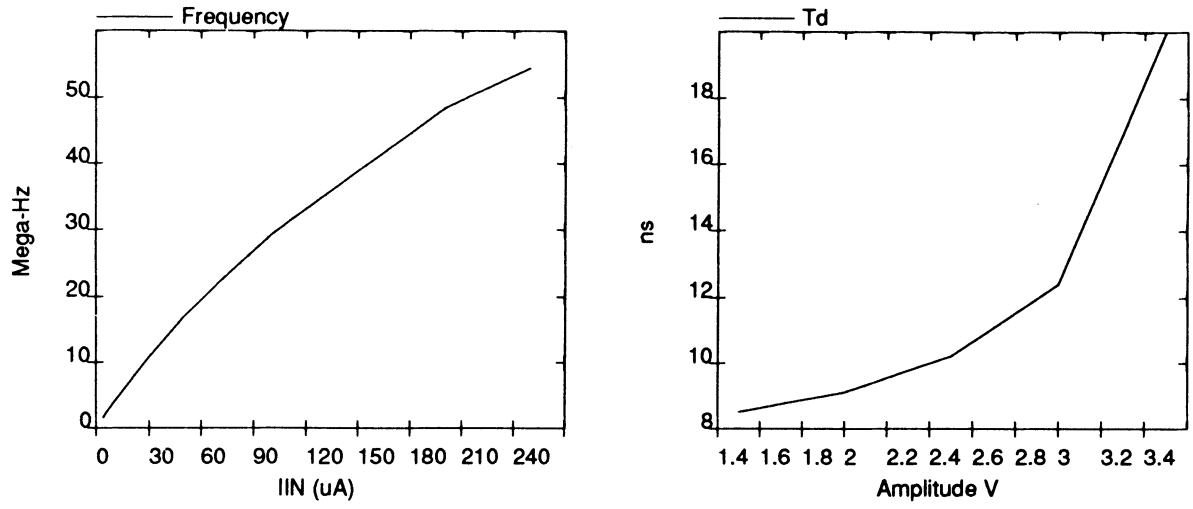

Figure 3: (a)Sample measured control characteristic, and (b) delay nonlinearity T_d.

The measured control characteristic of the oscillator running with a 1.5V amplitude is shown in figure 3. Frequency control over more than 6 octaves to frequencies in excess of 55MHz was achieved. The time delay nonlinearity T_d was determined for different capacitor voltage amplitudes and is also shown in figure 3. At the lowest amplitude T_d is only 8.5ns, the delay increases to 12.4ns when the amplitude is increased to 3V. This compares well with a recently published design, which when constructed in a high speed bipolar process ($f_T = 6GHz$) had a corresponding delay time of 16ns[3]. The temperature coefficient of a 10MHz output signal was determined over a -20°C to 120°C range. With the capacitor voltage amplitude set to 3.5V, the temperature coefficient was measured to be 390ppm/°C. The temperature coefficient drops to only 90ppm/°C when amplitude is lowered to 1.5V. Initial jitter measurements were made using a digitizing oscilloscope. For a 700KHz 3.5V waveform, jitter was determined to be less than 600ppm. However, it is likely that a substantial part of this jitter is due to triggering inaccuracy and thermal drift. Hand calculations, based on the work of Abidi and Meyer [1], point to a much lower figure.

5 Conclusion

A 5V CMOS controlled oscillator suitable for fine geometry processes has been described. The oscillator offers good control linearity of a low jitter, temperature stable, output. Because of its small size and simplicity the circuit should be a useful library element.

References

[1] A. Abidi and R. G. Meyer, "Noise in relaxation oscillators," *IEEE Journal of Solid State Circuits*, vol. 18, no. 6, pp. 794–802, 1983.

[2] M. H. Wakayama and A. Abidi, "A 30-MHz low-jitter high-linearity CMOS voltage-controlled oscillator," *IEEE Journal of Solid State Circuits*, vol. 22, no. 6, pp. 1074–1081, 1987.

[3] A. Sempel and H. van Nieuwenburg, "A fully-integrated HIFI PLL FM demodulator," in *Solid-state circuits conference - Digest of technical papers*, vol. 33, pp. 102–103, Feb. 1990.