A Fractional-N PLL modulator with flexible direct digital phase modulation

Mark Ferriss, David T. Lin, and Michael P. Flynn
University of Michigan
Ann Arbor, MI 48109, USA

***Abstract*- A 2.6GHz fractional-N synthesizer with a flexible digital modulation scheme is presented. The PLL output is modulated by adding a digital signal directly to the output of the phase detector, in contrast to the typical method of changing the divider ratio. A pre-emphasis filter is used to allow switching rates faster than the loop bandwidth. The transmitter supports GMSK, OQPSK, BSK or any constant envelop modulation scheme. Measurements are presented at 300kBit/sec. The 0.7mm^2 prototype in 0.13µm CMOS consumes 20mA from a 1.5V supply.**

I. Introduction

In this work, the output of a digital PLL is directly modulated by adding modulation information at the output of a digital phase detector. This is a more straightforward method of phase modulation, compared with the more typical, indirect method of adding modulation information to the frequency control of the divider. A prototype direct modulation 2.6GHz PLL is presented as a proof of concept. OQPSK and GMSK modulation schemes are demonstrated, and any constant envelop scheme can be supported. The digital PLL architecture is shown in Fig 1. On the left in Fig.1 is the phase detector loop, which was first introduced in [4]. This loop includes a phase quantizer, a digital integrator, and a feedback loop around a ΣΔ modulator and divider. A ΣΔ and a DAC converts the output of the digital integrator to an analog signal, which controls the tuning voltage of the VCO.

Section II explains how the gain of the digital-phase-detector is stable and predictable, modulation information added directly at the output of the phase detector causes a predictable phase change at the output of the loop. Pre-emphasis is used to compensate for the filtering effects of the PLL, allowing for faster modulation rates than the loop would otherwise allow.

In recent years, there has been an ongoing search for tools and techniques to replace analog-intensive components in frequency synthesizers with digital equivalents. For example, phase detectors with digital outputs have been proposed in [1],[2], and [3]. Typically, in a fractional-N modulator the phase of the output signal is indirectly modulated by changing the frequency control word at the ΣΔ input. In this work, because of the digital nature of the phase detector, digital phase modulation information can be added directly to the output of the phase detector, bypassing the ΣΔ and the phase detector. A local feedback loop around the phase detector controls the phase detector gain, so that adding phase modulation information at the phase detector output, results in a predictable phase change.

Traditionally, modulation data is added to the frequency-control-word input of the synthesizer, and the change in the phase of the PLL's output signal corresponds to the integration of this added signal. This is the preferred method for a conventional PLL, as it involves adding a digital signal to produce a phase change at the output.

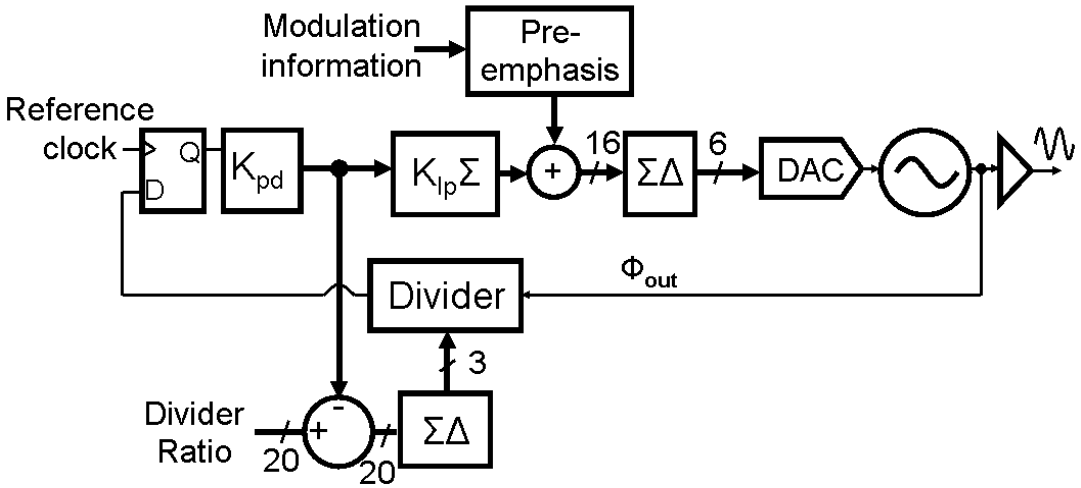

Fig. 1: Architecture of the PLL, including adding Pre-emphasis to the output of the phase detector.

An example of a more direct method to change the output phase is to insert a time delay in the reference path. This would also result in a phase change in the RF output, however the synthesis of accurate time delays is difficult, making this approach impractical.

The same effect can be produced by adding a signal at the output of the phase detector, which is equivalent to adding a time delay to the reference path, scaled by the phase detector gain.

The loop responds to a step added to the output of the phase detector by producing a phase change at the output of the PLL which returns the combined output of the phase detector and added signal to the original output of the phase detecor. This technique has two drawbacks if implemented in a conventional PLL: it requires accurate synthesis of currents to match the charge pump currents, and assumes precise knowledge of the phase detector gain. In this work, a digital phase detector with a well-controlled gain is used, therefore digital modulation information can be added directly to the output of the phase detector without the need for the synthesis of accurate currents.

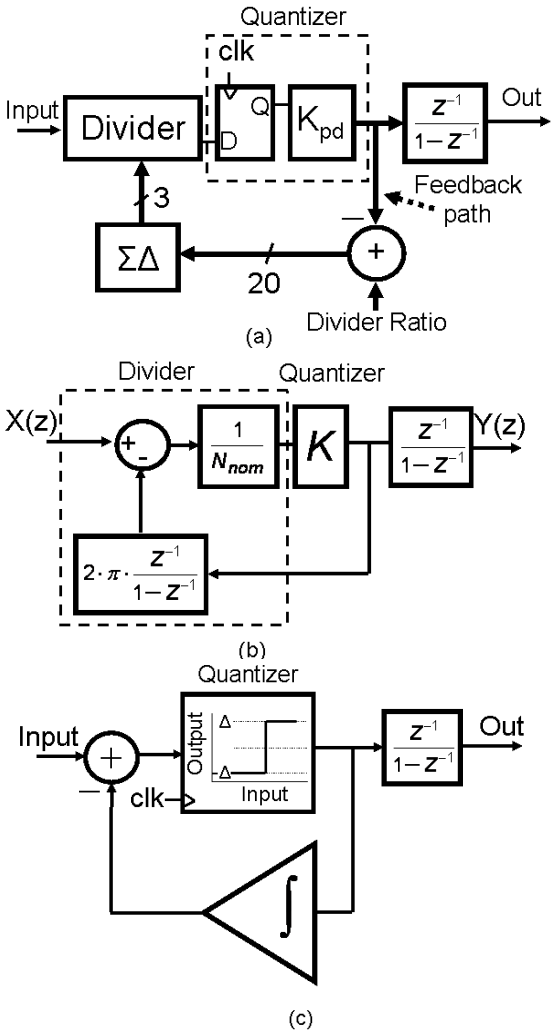

Fig. 2: (a) A Phase to digital converter based on a delta modulator. (b) Z domain model. (c) A standard delta modulator

II. Phase Detector Overview.

In this section a phase detector, with a well controlled gain, first presented in [4] is discussed. Adding digital phase information to the output of the PD results in a well-defined phase change at the output. (Adding digital modulation information directly to the output of the phase detector has also been demonstrated in an all-digital PLL with TDC based phase detector [5].)

A block diagram of the phase detector is shown in Fig. 2(a). The input on the left is the high frequency RF signal from the VCO. A single flip-flop is used as a phase quantizer, and the quantized phase information is then fed back to the input of the ΣΔ controlled divider. A small signal phase domain model is shown in Fig. 2(b). This architecture behaves much like a delta modulator (Fig. 2(c)), which consists of a feedback loop with a quantizer in the forward path, and an integrator in the feedback path. One of the defining characteristics of a delta modulator is that the integrator in the feedback path ensures that the average of the feedback signal equals the average of the input signal, irrespective of the gain of the quantizer. This means that if the gain of the feedback path is known, then the low frequency gain of the overall system is also known. In this phase detector model in Fig. 2(b), the integration in the feedback path is caused by feeding quantized phase information back to the frequency control of the divider. As phase is the integration of frequency, this implies there is a digital integrator in the feedback path. A z domain model for the system is shown in Fig. 2(b). In the model the input, X(z), corresponds to RF signal (the output of the VCO). Even though the RF signal itself is a continuous time signal, its phase is effectively sampled on the edges of the reference clock, so it is appropriate to model it as a sampled signal. Y(z) corresponds to the output of the phase detector. The phase detector gain is given as K. It is straight forward to show that:

$$\frac{Y(z)}{X(z)} = \frac{K/N_{nom}}{(1-z^{-1})/z^{-1} + K/(N_{nom}2\pi)} \quad (1)$$

When z=1, giving the DC response, the net result is Y(1)/X(1)=1/2π. Hence the DC gain of from the VCO output to the integrator output is independent of the feed forward gain, which includes the phase detector gain. The other elements of the model are well defined and stable. For these reasons, the gain of the quantizer is stable and easily calculated. If modulation information is added directly to the output of the phase detector then the loop responds with a phase change in order to cancel out this added signal. Because the gain of the overall PD is known, this results in a predictable phase change at the output.

III. Pre-emphasis filter.

Another challenge with modulation in fractional-N synthesizers is that the modulation can be distorted by the filtering characteristics of the PLL loop. Pre-emphasis filters are often used to compensate for this filtering action [6], but

the effectiveness of pre-emphasis is limited if the pre-emphasis filter does not match the transfer function of the loop due to PVT variations. With the proposed digital phase detector, which has a known low frequency gain, the VCO is the only block with a PVT dependant gain, therefore the low frequency characteristics of the loop are less susceptible to PVT variations and easier to match with a pre-emphasis filter.

In this work, the pre-emphasis filter consists of a digital IIR filter as shown in Fig 3. The PLL is a type 1 system. The dominant pole of the PLL is compensated with the pre-emphasis filter, and higher order poles are ignored. A bi-linear transform was used to transform a simplified (single pole) approximation of the PLL's transfer function into a form that can be fitted to the z domain filter in equation (2) and in Fig. 3. Higher order poles where ignored.

$$\frac{out(z)}{in(z)} = \frac{B_0 + B_1 z^{-1}}{1 - A_1 z^{-1}} \qquad (2)$$

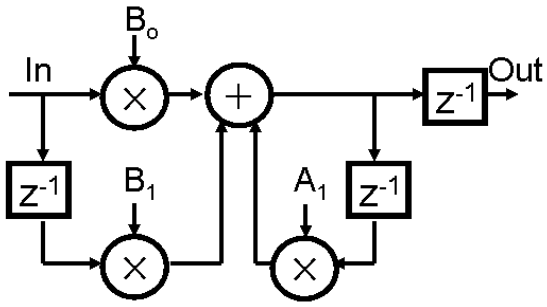

Fig. 3: Digital pre-emphasis filter.

IV. Physical Prototype.

A prototype is manufactured in 0.13µm CMOS, and occupies an active area of 0.7mm^2 (Fig. 9). The on-chip digital circuitry includes the digital pre-emphasis filter, the ΣΔs used in the programmable divider and DAC, and all of the other digital shown in Fig. 1. The analog section consists of the DAC, VCO and output buffers. The digital circuitry including the phase detector is implemented using digital standard cells. The only analog circuitry required is the on-chip DAC and VCO. The prototype draws 20mA from a 1.5V supply, with an additional 10mA used in the output buffer.

V. Test Setup and Measurement Results.

In Fig. 4 an overview of the test setup is shown. The transmission filter is implemented externally on an FPGA, which communicates with the prototype I.C. over an SPI port. The SPI port can also be used to program the loop gain constant K_{lp}, and hence to change the loop bandwidth.

The output spectrum without modulation is shown in Fig 5. In Fig. 6 the output phase noise is shown with different loop bandwidth configurations. The phase detector's quantization noise dominates for the loop bandwidths shown here. The phase detector quantization noise is flat versus frequency, and is subsequently filtered by the low-pass characteristic of the loop. This explains why reducing the loop bandwidth reduces the phase noise above the loop bandwidth.

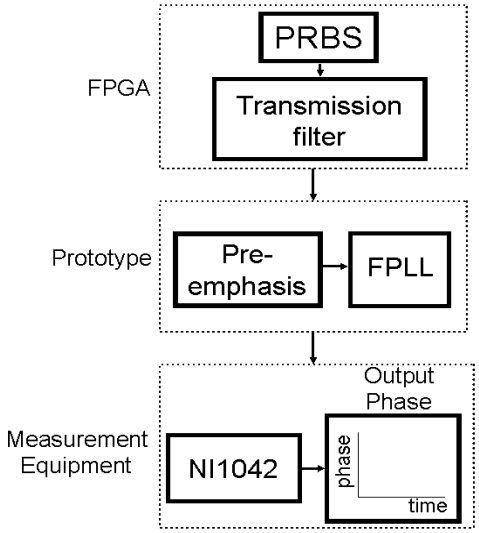

Fig. 4: Overview of the test setup.

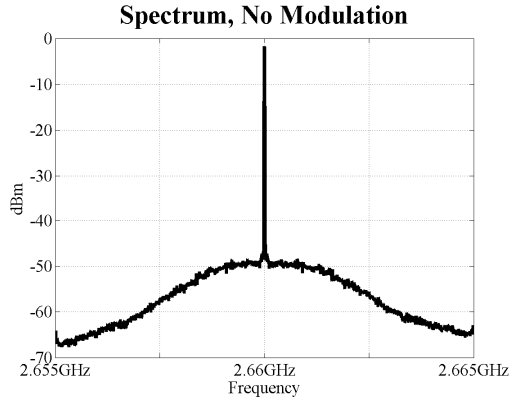

Fig. 5: Output spectrum without modulation.

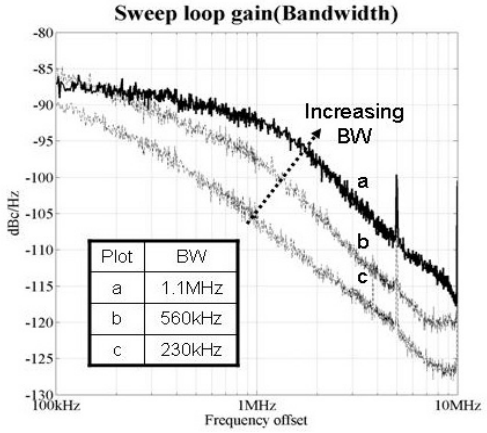

Fig. 6: Phase noise for different loop BW settings.

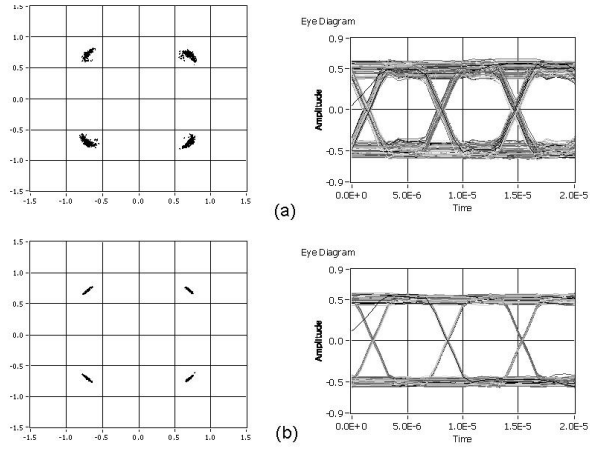

Fig. 7: 300kbit/s OPPSK constellation and eye diagrams. (a) Without pre-emphasis (b) With pre-emphasis.

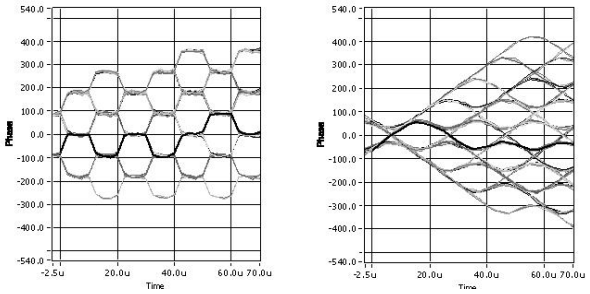

Fig. 8: Trellis diagram (a) OQPSK (b) GMSK.

Fig. 7 shows measured constellation and eye diagrams for OQPSK modulation, with pre-emphasis turned on and off. In this experiment the transmission rate is 300kbits/s. As can be seen from Fig. 7, turning on the pre-emphasis filter results in a significant improvement in the constellation diagram. The pre-emphasis filter compensates for only the dominant pole of the loop. A more sophisticated pre-emphasis filter which includes some of the higher order poles would improve the results ever further. Fig. 8 shows trellis diagrams for both OQPSK and GMSK at 100kbits/s.

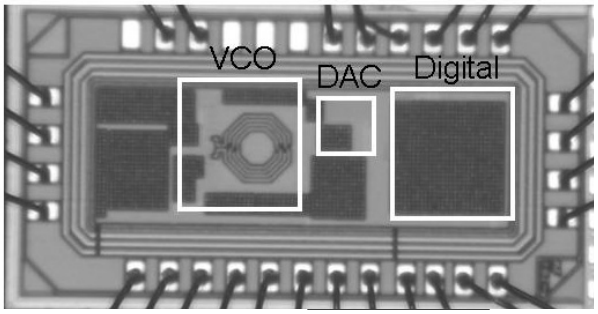

Fig 9: Die micrograph.

VI. Conclusion

In this work a new method for modulating the output phase and frequency of fractional-N synthesizer has been demonstrated. An oversampled single-bit phase detector was shown to produce a stable, predictable gain provided that it was within a delta modulation feedback loop. This allowed digital phase modulation information to be added directly to the output of the phase detector. All concepts were demonstrated in a physical prototype.

Total current	20mA (+10mA in output buffer)
Active (and total) area	0.7mm2 (2mm2)
Modulation schemes	QPSK, BPSK, GMSK
Output frequency	2.66GHz
Phase noise @1MHz, with bandwidth of 230kHz, 560kHz, 1.1MHz	-107dBc/Hz, -97dBc/Hz, -92dBc/Hz
Reference clock	250MHz
Loop type, order	1, 4

Table 1: Performance Summary

References

[1] R. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg and P.T. Balsara, "1.3V 20ps time-to-digital converter for frequency synthesis in 90-nm CMOS," IEEE Transactions on Circuits and Systems II, vol. 53, Issue 3, pp. 220–224, March 2006.

[2] C.M. Ming, M. Z. Straayer, M.H. Perrott "A Low-Noise, Wide-BW 3.6GHz Digital ΔΣ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation", ISSCC Dig. Tech. Papers, pp. 340–341, 2008.

[3] R. Beards and M. Copeland, "An oversampling delta-sigma frequency discriminator," IEEE Transactions on Circuits and Systems II, vol. 41, no. 1, pp. 26 – 32, January 1994.

[4] M. Ferriss and M. P. Flynn, "A 14mW Fractional-N PLL modulator with an enhanced digital phase detector and frequency switching scheme" ISSCC Dig. Tech. Papers, pp. 353–353, 2007.

[5] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Verrulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammed, and D. Leipold, "All-digital PLL and transmitter for mobile phones," IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[6] M.H. Perrott, "Techniques for High Data Rate Modulation and Low Power Operation of Fractional-N Frequency Synthesizers", Ph.D. dissertation, MIT, Cambridge, MA, 1997.