A 12b 11MS/s Successive Approximation ADC with two comparators in 0.13µm CMOS

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Abstract

A two-comparator architecture, incorporating deliberate comparator offset and pre-amplifier power management, reduces comparator meta-stability and comparator power consumption in a 12b 11MS/s SAR ADC. A prototype, fabricated in 0.13µm CMOS achieves an FOM, SNDR, SFDR and error rate of 311fJ/conversion step, 62.4dB and 72.8dB and $<1.9\times10^{-12}$, respectively, at 11MS/s.

Keywords: SAR ADC, two-comparator architecture.

Introduction

Moderate-resolution (<10b) SAR ADCs have achieved state-of-the-art power performance in fine-line CMOS technologies [1-3]. However, due to the nature of the successive approximation algorithm, the SAR comparator may have to resolve a very small voltage during any conversion cycle. For example, if the input is half full scale, there is a risk of metastability in the second decision. To reduce the risk of metastability, a two-comparator architecture is proposed. The two-comparator architecture incorporates a deliberate comparator offset which reduces the risk of metastability without increasing comparator gain or adding comparator latency. An integer-based, non-binary redundancy technique simplifies the SAR logic and provides redundancy for the two-comparator scheme. Comparator pre-amplifier power management exploits redundancy to further reduce power consumption.

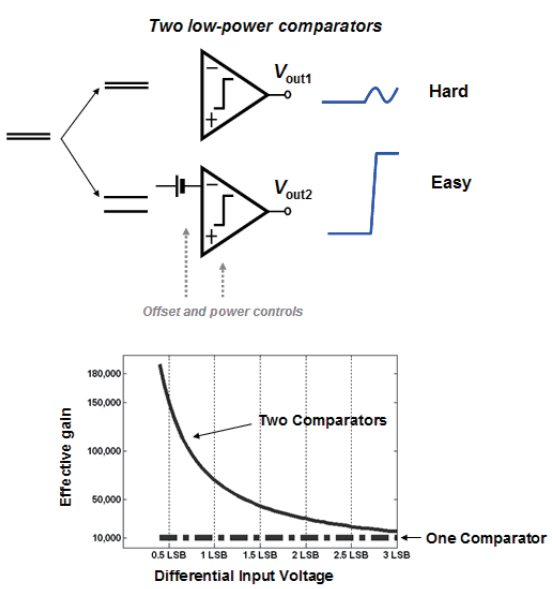

Fig. 1: Use of two comparators greatly increases the effective gain.

Two Comparator Architecture

During the first five of thirteen approximation cycles, two low-power, low-gain comparators are used instead of a single comparator. The two comparators, which compare the top-plate nodes of the capacitor DAC, are deliberately offset by 8LSBs. As a result of this deliberate offset, the effective input voltage of at least one of the comparators is always greater than 4LSBs, thus greatly increasing the effective gain of the comparators. For example, for a 0.01LSB voltage input, the effective input of one comparator becomes 4.01LSB, so that the effective gain is 400 times larger. The graph in Fig 1 shows the effective gain using the two-comparator scheme. The effective regenerative gain increases greatly when the input is smaller than 4LSB. The comparator that makes the faster decision controls the next step in the SAR algorithm. In this way, the probability of comparator metastability is reduced and ADC error-rate is improved without additional comparator latency or gain.

A timing diagram for the two-comparator operation is shown in Fig. 2. Each comparator incorporates a pre-amplifier, which reduces both kick-back and the input-referred noise of the comparator's regenerative amplifier. The preamplifier can be completely shut off, or can be operated either in low-noise mode (1mA) or moderate-noise mode (0.2mA). During the first five SAR cycles, the two comparators are configured in moderate-noise mode and an 8LSB offset is introduced by the pre-amplifier trim DACs. During this time, the pre-amplifiers operate in moderate-noise mode to save power consumption since the accuracy requirement is relaxed thanks to redundancy. For the remaining cycles one comparator is configured in low-noise mode while the other comparator is shut off. The offset of the comparator is set to offset-nulled value, which is determined at power-on.

An integer-based non-binary arbitrary-radix redundancy scheme is adopted to relax noise and settling requirements and to simplify the SAR logic. The integer-based radix simplifies the digital logic and reduces power consumption by eliminating the need for a conversion table or a multiplier usually required

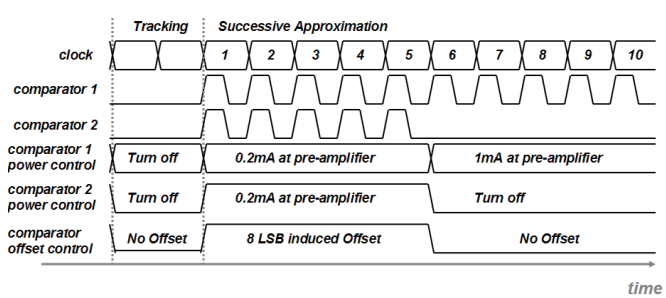

Fig. 2: ADC operational timing diagram.

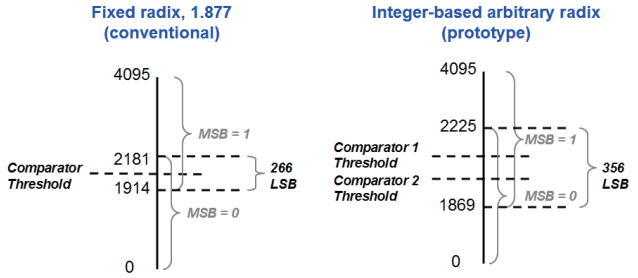

Fig. 3: Redundancy in conventional fixed radix and in an integer-based, arbitrary, non-binary radix.

in a fixed radix scheme [4]. However, the method is modified to provide more redundancy in the first five cycles to facilitate the offset two-comparator scheme. The arbitrary-radix used in this prototype moves some redundancy from later cycles to earlier cycles, while maintaining the required DAC settling time for each cycle equal to or less than the maximum required DAC settling time for a 1.877 fixed radix. For the last three cycles, a binary radix is used since these cycles require less DAC settling time than the clock period. A 1.877 fixed non-binary radix, that represents 12b with 13 SAR cycles, provides a redundancy of 266LSB for the MSB decision, as shown on the left side of Fig. 3. Instead, the weighted integer-based arbitrary radix provides a redundancy of 356LSB for the MSB decision, as shown in the right side of Fig. 3. The relaxed MSB accuracy requirement allows the use of two offset comparators during the first five SAR cycles.

Trim DACs in the preamplifier both correct comparator offsets and introduce deliberate offsets in the comparators. During power-on, the DACs correct comparator offsets to within one-half LSB. The trim DACs force a controlled offset of 8LSBs between the comparators while the ADC is operating in two-comparator mode during the first 5 SAR cycles; afterwards the offset returns to the power-on offset-nulled value.

To reduce latency, the digital block pre-calculates the next two possible values of the DAC driving registers. An adder and a subtractor pre-calculate the non-binary approximation, and the comparator which decides first determines which of the two pre-calculated DAC driving registers is applied. A comparator 'done' signal triggers the digital block to drive the DAC immediately once the comparator decision is made to provide additional DAC settling time [5].

Measurement Results

A prototype 12b 11MS/s SAR ADC is fabricated in 0.13µm CMOS and has an active area of 0.7mm^2. A micrograph of the chip is shown in Fig. 4. The measured DNL and INL at 11MS/s are plotted in Fig. 5, and are within 0.8LSB and 3.0LSB respectively, without capacitance calibration. The measured SNDR and SFDR are 63dB and 70dB, respectively, for a Nyquist input at 11MS/s. The prototype consumes 0.97mW from a 1.0V analog supply and 2.6mW from a 1.0V digital supply. The power consumption of the ADC driver, pad drivers, and two external reference voltages are not included in this calculation. The digital power consumption is 1.9mW at 8MS/s and 0.91mW at 3MS/s. The figure-of-merit for the prototype is 311fJ/conversion.step at 10MS/s. The figure-of-merit is less than 400fJ/conversion.step over the wide operational range from 3MS/s to 11MS/s and a minimum of 278fJ/conversion.step is achieved at 9MS/s. The word-error-

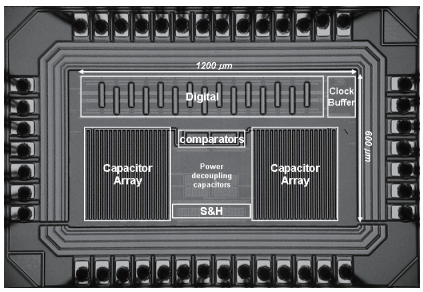

Fig. 4: Die microphotograph of 12b prototype.

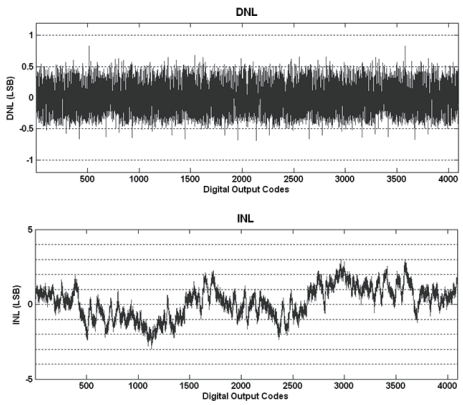

Fig. 5: Measured DNL and INL at 11MS/s.

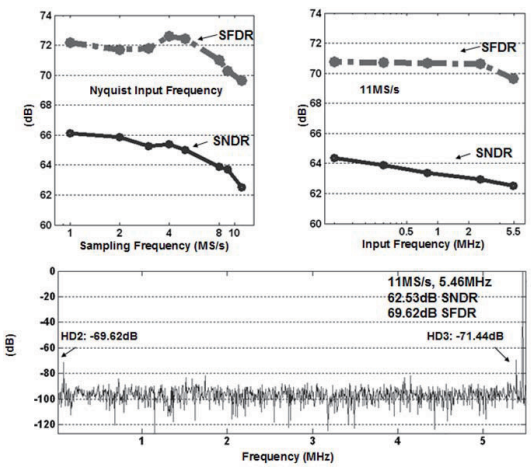

Fig. 6: ADC dynamic performance.

rate of the ADC at 11MS/s, measured with the method proposed in [6], is less than 1.9×10^{-12}.

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