9.4 A 9b 14μW 0.06mm² PPM ADC in 90nm Digital CMOS

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As CMOS dimensions scale down, time-domain resolution of digital signals improves but the voltage resolution of analog signals degrades [1]. In this paper, we introduce an ADC architecture based on Pulse Position Modulation (PPM), which relies more on time resolution than on amplitude resolution. In PPM (Fig. 9.4.1(a)), a continuous-time comparator compares the input signal with a voltage ramp. The time interval between the ramp starting point, which is synchronous with the reference clock, and the instant the input signal crosses the ramp (i.e. [t_1, t_2, t_3, ...] in Fig. 9.4.1(a)) is measured by a 2-step time-to-digital converter. Assuming the ramp slope is constant, we can calculate the input-signal amplitude from the measured time vector.

Unlike a conventional ADC, the PPM ADC samples the input non-uniformly. An oversampling ratio of 8× or higher is required if a traditional linear recovery technique such as low-pass filtering, is used to reconstruct the original analog input signal in PWM or PPM [2]. Instead, we rely on a time-varying/nonlinear recovery technique to sample the signal at a frequency close to the Nyquist rate [3], with an oversampling ratio of 1.7×. This way we can sample higher input frequencies with lower power consumption, at the cost of more complexity in digital post processing.

The main signals in the PPM ADC are shown in Fig. 9.4.1(b), and a block diagram of the ADC is shown in Fig. 9.4.2. A 128MHz reference clock is divided by a chain of flip-flops to provide a 1MHz *start* signal that controls ramp generation. When the ramp voltage becomes greater than the input signal, an unclocked comparator generates a *stop* signal. A time-to-digital converter (TDC) measures the time (t_m in Fig. 9.4.1(b)) from the start of the ramp (*start* rising edge) to the point at which input signal and ramp intersect (*stop* rising edge). A 2-step TDC [4,5] is used to simultaneously achieve a large dynamic range and fine time resolution.

A coarse time quantizer, formed with a counter, measures the number of reference clock cycles between the start of the ramp and the *stop* signal. To avoid metastability and setup issues, this coarse time measurement (t_c) is made to the 2nd-next reference clock rising edge after the *stop* signal rising edge. The fine ADC measures the time t_f between the *stop* signal and the 2nd-next reference clock rising edge after *stop* and the overall TDC output is $t_m = t_c - t_f$.

The TDC is shown in Fig. 9.4.3. The synchronizer selects the 2nd rising edge of the reference clock after the *stop* signal as the *clk_stop* signal. The *stop* signal is an asynchronous signal that arrives at an unknown phase with respect to the reference clock, and measurement to *clk_stop* ensures that the flip-flop setup time is satisfied. The synchronizer also generates a *counter_enable* signal that is synchronously set by *start* and asynchronously reset by *clk_stop*. In this way the coarse time measurement made by the counter is correctly stitched to the fine time measurement. From the input range and ramp slope, the maximum time interval is 250ns so that a 128MHz counter resolves 5 MSBs.

A fine sub-TDC measures the interval, t_f, from the *stop* rising edge to the *clk_stop* edge. A 32-element delay line is tuned to generate 32 delay steps covering 2 full periods of the reference clock. Two delay periods are required since the synchronous *clk_stop* signal is the 2nd-next reference clock edge after the comparator *stop* signal. The asynchronous comparator output signal, *stop*, is the input to the delay line. 32 flip-flops, each clocked by the *clk_stop* signal, sample delayed versions of the *stop* signal. The outputs of these flip-flops form a thermometer code with the number of 1's indicating the distance in time from *stop* to *clk_stop*. A Wallace-tree encoder suppresses bubbles and sparkles in the thermometer code. Running the interpolating delay line off the *stop* edge and not off the reference clock saves power, since the delay cells are only activated when there is a comparator transition. As the 32 delays cover 2 reference clock periods, the fine ADC resolves 4 LSBs.

The delay line is composed of 32 current-starved buffers, where the gate voltage of the footer devices is controlled by tuning voltage (V_c), as shown in Fig. 9.4.3. The delay buffers are calibrated during a calibration cycle in which a half clock rate is applied to the interpolator and the V_c is tuned to activate all 32 sampler flip-flop outputs. The control voltage versus delay characteristic covers the full PVT range. Additional delay stages are added at the tail of the 32 buffer chain to detect buffer overflow errors. The delay sampling flip-flops are sense-amplifier flip-flops adapted from [6].

The ramp generator and the continuous-time comparator are shown in Fig. 9.4.4. The ramp generator consists of a cascoded current source charging a constant capacitance under the control of digital switches. Since the input signal is compared with the ramp only during charging, there is no requirement to match charging and discharging rates and capacitor discharge is achieved simply with a switch to ground. Simulations indicate that a linearity of 11b is achieved over a 600mV ramp range. The transistor lengths are large to reduce flicker noise.

The continuous-time comparator consists of a PMOS input differential amplifier followed by a common-source stage. Input-stage transistor sizes are chosen to limit propagation delay variation over the input common mode range to less than one LSB of the TDC time measurement. Noise in the ramp and comparator circuits causes timing jitter, limiting the accuracy of time measurement [7]. Increasing the ramp slope reduces jitter but limits input dynamic range.

The PPM ADC is a hybrid synchronous/asynchronous architecture. Unlike the case with an asynchronous ADC [8,9], different reference levels and comparators are not required since the ramp sweeps the entire input voltage range. In addition, the use of a single comparator eliminates consideration of comparator offset and mismatch. Unlike in [10], the use of a clock synchronous ramp signal removes the requirement for asynchronous digital protocols, reducing power consumption and area. Unlike a single slope ADC [11,12] the input signal is continuously compared with the ramp input, eliminating the sample-and-hold circuitry.

The prototype is fabricated in 90nm digital CMOS and occupies 0.06mm². The analog circuits run off a 1V supply and the digital blocks operate at near-threshold from a 400mV supply. The input-signal bandwidth is 300kHz and the measured ENOB is 7.9b for f_S=1MHz over the entire bandwidth. The measured power consumption of the entire system is 14μW (excluding digital post-processing). The figure-of-merit, defined as

$$\left(\frac{power}{2 \times BW \times 2^{ENOB}}\right),$$

is 98fJ/conversion-step. The measured spectrum for a 40.25kHz tone sampled at f_S=1MHz is shown on top of Fig. 9.4.5. The FFT of the raw non-uniform data shows large harmonics due to non-uniform sampling. The spectrum of the same signal after the iterative algorithm is applied creating uniform samples in post-processing (bottom of Fig. 9.4.5) shows that these artifacts are suppressed and the SNDR and SFDR are improved. DNL, INL and SNDR vs. f_{in} are shown in Fig. 9.4.6.

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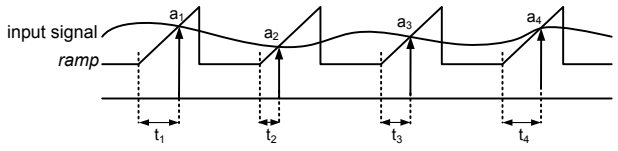

Figure 9.4.1(a): PPM modulation.

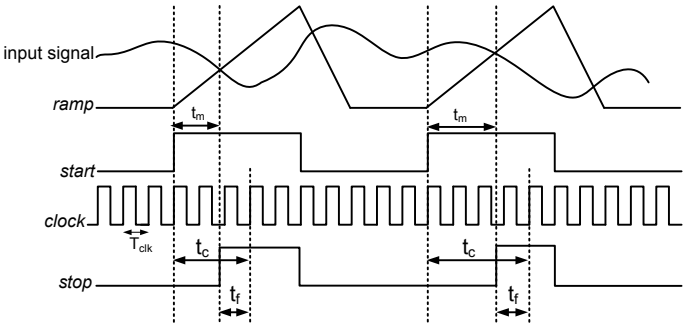

Figure 9.4.1: (a) PPM modulation, and (b) PPM ADC signals.

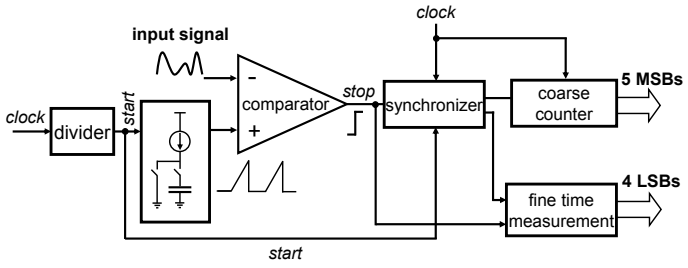

Figure 9.4.2: ADC block diagram.

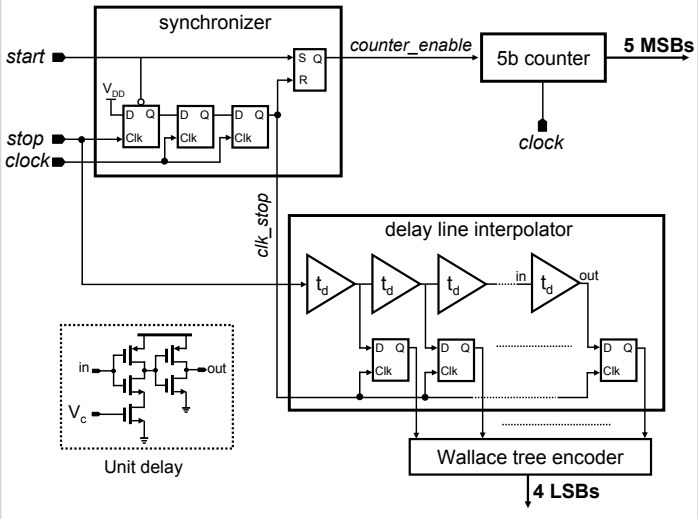

Figure 9.4.3: TDC block diagram.

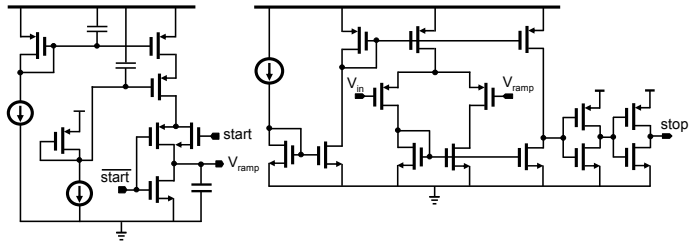

Figure 9.4.4: Ramp generator and continuous-time comparator.

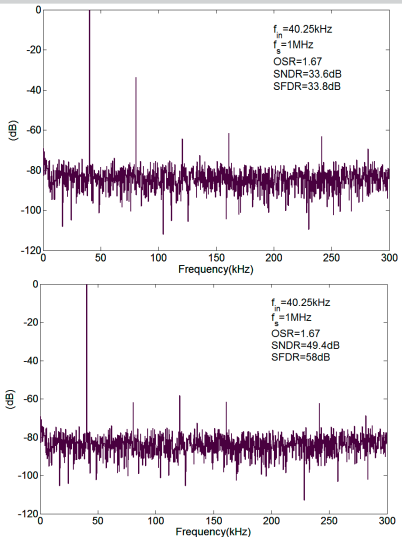

Figure 9.4.5: Measured spectrum of a single tone at 40.25kHz before post-processing (top) and after post-processing (bottom).

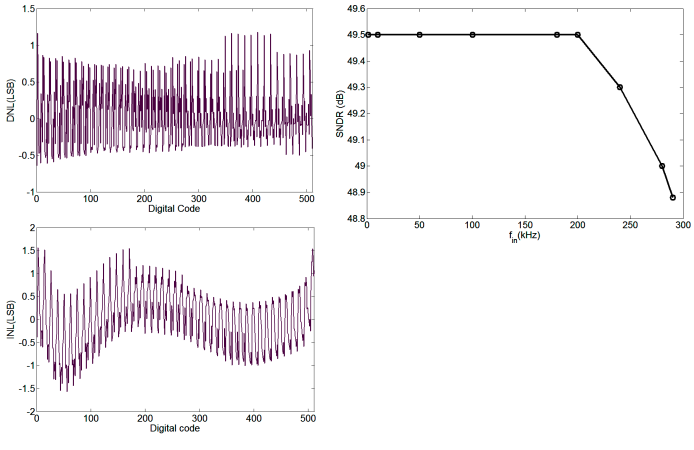

Figure 9.4.6: Measured DNL, INL and SNDR versus f_{in} at f_S=1MHz.

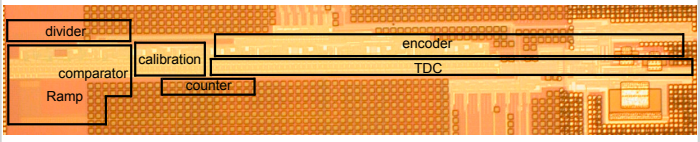

Figure 9.4.7: Die micrograph.

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