A 14 mW Fractional-N PLL Modulator With a Digital Phase Detector and Frequency Switching Scheme

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***Abstract*—In this work an all-digital phase detector for a fractional-N PLL is proposed and demonstrated. The phase detector consists of a single flip-flop, which acts as an oversampled 1 bit phase quantizer. A digital sampling scheme that enables FSK modulation rates much larger than the loop bandwidth is demonstrated, without compromising on the frequency accuracy of the output signal. A prototype 2.2 GHz fractional-N synthesizer incorporating the digital phase detector and sampling scheme is presented as a proof of concept. Although the loop bandwidth is only 142 kHz, an FSK modulation rate of 927.5 kbs is achieved. The 0.7 mm^2 prototype is implemented in 0.13 μm CMOS consumes 14 mW from a 1.4 V supply.**

***Index Terms*—ADC, DAC, delta-sigma, fractional-PLL (FPLL), fractional-N, FSK, phase minimization loop, phase-locked loop (PLL), PML, synthesizer.**

I. Introduction

THE fractional-N frequency synthesizer is a key building block of wireless systems as it can both generate a high frequency signal with a well defined frequency and modulate that signal [1], [2]. An introduction to the use of $\Sigma\Delta$ modulator in frequency synthesis can be found in [3], and a block diagram of a conventional fractional-N synthesizer is shown in Fig. 1. The popularity of this architecture is derived from its ability to do much of the signal processing required for control of the output frequency in the digital domain. Nevertheless, this architecture still relies on a significant amount of analog circuitry. The design of analog circuits in the deep submicron (DSM) age is challenging, and can often lead to excessive power dissipation, increased sensitivity to substrate/power supply noise, and to sensitivity to process variation which can compromise performance or yield. Many of these problems are evident in fractional-PLL (FPLL) design. Charge pumps require good matching between currents of opposite polarity. Low loop-time-constants are typically required, so the loop filter must be implemented using large area capacitors or expensive off chip components. Furthermore, these blocks do not take advantage of the major strength of DSM processes, which is the ability to build fast, complex, low-power digital signal processing circuits.

Another challenge associated with the FPLL architecture, is the difficulty of achieving high-speed modulation of the RF output signal. The $\Sigma\Delta$ modulator used to control the divider injects high-pass-shaped quantization noise into the loop, but the PLL itself has a low bandwidth, which naturally rejects the high frequency portion of the $\Sigma\Delta$ noise. However, the average divide ratio should be modulated at a rate less than the PLL bandwidth, otherwise the modulation signal is filtered by the PLL's low-pass characteristic. On the other hand, if the PLL bandwidth is widened to accommodate faster modulation, any reference jitter and/or $\Sigma\Delta$ quantization noise undergoes less filtering, degrading the phase noise of the output signal.

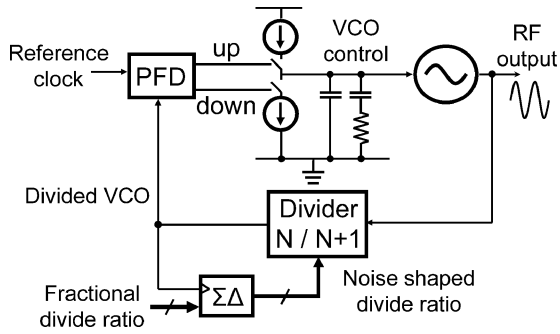

Fig. 1. Conventional fractional-N synthesizer.

Several techniques have been proposed to overcome these shortcomings; however many of these have limitations. In pre-emphasis, the frequency control signal is passed through a transfer function that is the inverse of the PLL's, in order to compensate for the effects of the PLL filtering. This technique can compensate for the limited loop bandwidth [4] but requires knowledge of the loop's frequency response. Another method is two-point modulation, where in addition to modifying the divide ratio, a modulation signal is added directly at the input of the VCO [5]. However, unless the value of the injected signal exactly corresponds to the VCO gain, the frequency step size is incorrect, although the loop will eventually settle to the correct frequency. Least mean square (LMS) based gain calibration techniques show promise, these can also have slow associated time constants [6]. In [7], the VCO control path is cleverly split into two: a common mode path for the VCO, and a differential mode path for the LMS algorithm. This allows the LMS speed to be set independently of PLL bandwidth. LMS based schemes have also been successfully used in TDC based all digital PLLs [8].

In this paper we propose and demonstrate techniques which address two limitations of the FPLL modulator architecture; the reliance on analog circuitry in deep-submicron technology, and the trade off between low loop bandwidth for good $\Sigma\Delta$ noise rejection, and high loop bandwidth for fast modulation rates [9].

Manuscript received November 16, 2007; revised May 11, 2008. Current version published November 19, 2008. This work was supported in part by the WIMS Engineering Research Centers under NSF Award Number EEC-9986866, and in part by Intel.

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Digital Object Identifier 10.1109/JSSC.2008.2005435

Section II introduces an all-digital phase detector, which relies on a single flip-flop for phase quantization. Section III introduces a simple digital dual-modulation scheme that alleviates the tradeoff between loop bandwidth and switching speed, for FSK modulation schemes. Section IV discusses additional implementation details, and finally Section V discusses measured results and conclusions.

II. Digital Phase Detector

An FPLL system can be considered to be a type of digital-to-analog or more specifically a digital-to-frequency converter, with the phase of the input clock acting as the reference, the frequency of the input clock corresponding to the sampling rate, the divider control corresponding to the digital input, and finally the frequency of the RF signal corresponds to the output. It should come as no surprise that many of the challenges associated with building these systems in deep sub micron (DSM) processes are similar to the challenges associated with ADC/DAC design. In this work we employ converter design techniques in order overcome some of these limitations.

A block diagram of a conventional fractional-N synthesizer can be seen in Fig. 1. The information extracted by the phase detector is inherently analog in nature, since the phase information is not synchronized to either the reference clock or the divided down VCO clock, and is not quantized. Although conventional XOR and tristate phase detectors utilize digital building blocks, a charge pump and filter are still required to extract useful phase-difference information. In [11] a time-to-digital converter (TDC) uses multiple flip-flops and unit delays (in practice inverters) to quantize the time difference between the edges of the reference clock and feedback clock. With this approach, resolution and linearity are dependant on the speed and matching of the unit delay elements, and hence inherently process dependant.

If a conventional TDC is analogous to a flash ADC, with the unit delays setting the quantization steps, then the proposed phase detector is analogous to an oversampling ADC, with oversampling and a phase integration loop used to improve the performance of a coarse single-bit phase quantizer. To achieve this we utilize a unique property of a fractional-N PLL, that is the ability to control the frequency of the signal coming from the programmable divider by changing the divide ratio.

The proposed phase detection technique uses a single flip-flop as a phase comparator, while an additional negative feedback loop around the programmable divider keeps the phases of the two clocks aligned to within a single quantization step. On the rising edge of the reference clock, the flip-flop samples the divided-down VCO signal, determining whether the divided clock is ahead or behind the reference clock. In this way, the flip-flop effectively acts as a one-bit phase quantizer. In Fig. 2 a single flip-flop is used to quantize the phase difference, $\Delta\Phi$, between the reference clock and the divided down VCO clock. The quantization noise of the $\Sigma\Delta$ controlled divider is added to the divided down VCO clock and this acts as dither for the phase quantizer. If this dither were absent, and for example if $\Delta\Phi$ is positive, then the output of the flip-flip (quantizer) would always be one, irrespective of the magnitude of phase difference between the divided down clock and reference clock. In the presence of the dither, the output of the flip-flop is sometimes one and sometimes zero. Similar to an oversampled ADC, the low-pass-filtered output of the flip-flop is proportional to $\Delta\Phi$. An approximately linear relationship is achieved if the phase difference $\Delta\Phi$ can be kept small relative to magnitude of dither.

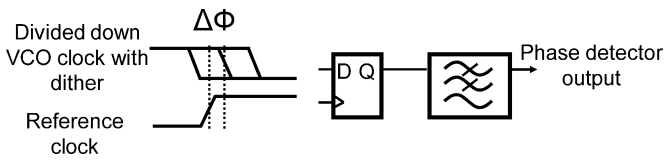

Fig. 2. Using a flip-flop as a phase quantizer.

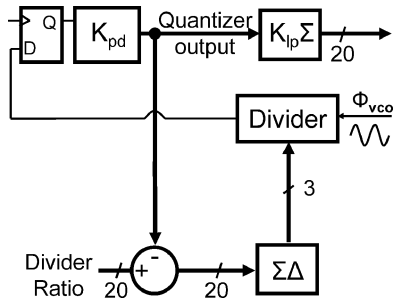

Fig. 3. New phase detector configuration with the phase minimization loop (PML).

Single bit quantized phase detectors can also be found in Bang-Bang PLLs. In a Bang-Bang PLL the output signal typically goes directly to the phase detector (or through a static divider), hence the phase of the PLL output or PLL input signal must change if the output of the phase quantizer is to change [10]. Therefore in a Bang-Bang PLL, the phase quantizer can only provide information on the polarity of any phase difference between the system input and output. In contrast, in this work the VCO output passes through a $\Sigma\Delta$ controlled programmable divider before it reaches the phase-detector. This means that by changing the divide value, the phase quantizer is exercised in the absence of any change in excess phase of the VCO output. The $\Sigma\Delta$ also provide dither to the phase quantizer, an important requirement for any oversampled quantizer.

An additional inner feedback loop, seen in Fig. 3, is introduced to keep the phase difference between the two clocks small, i.e., minimizing $\Delta\Phi$. For this reason the new loop is called the *phase minimization loop* (PML). This phase feedback scheme might be recognized as being similar in form to a *delta modulator*, a commonly used ADC/DAC architecture. In a delta modulator the forward path consists of a quantizer, and the feedback path includes an integrator. (In this work the integration occurs because phase information is fedback to the frequency control of the divider.) The integrator keeps the phase difference at the input of the quantizer small. Although the overall PLL keeps the average of $\Delta\Phi$ at zero, the instantaneous value of $\Delta\Phi$ is a function of the bandwidth of the PLL, which cannot be set arbitrarily large. The bandwidth of the inner loop, however, can be set to be larger than that of the overall PLL, hence can do a better job keeping the two clocks in close phase alignment. This is necessary in order for the phase detector to behave in an approximately linear fashion. If the phase

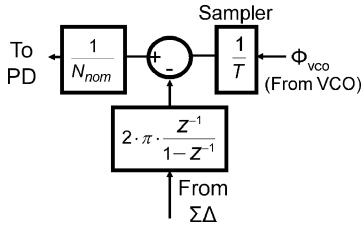

Fig. 4. Small-signal model of the divider.

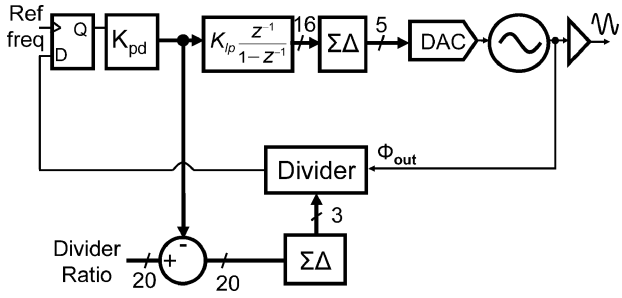

Fig. 5. Overall architecture for proposed FPLL.

deviation, $\Delta\Phi$, is too large then the quantizer output becomes stuck at 1 or -1, and the dither will not have the desired effect. The one-bit output of the flip-flop is passed through a linear scaling block $K_{\rm pd}$, so that the output of the quantizer is $\pm K_{\rm pd}$. $K_{\rm pd}$ is used to set the quantizer step size. A similar technique is presented as part of a frequency discriminator[1] in [13], which can be used as an RF demodulator or as part of a Fractional-N PLL [14], [15][2], in which the quantized phase signal is fed directly back to the divider control, and there is no $\Sigma\Delta$ in the feedback path.

The only pseudo-analog component is the decision making flip-flop, while everything else is synchronous digital circuitry. The flip-flop should be treated in a similar fashion to a comparator in an ADC, as its set-up and hold times are not necessarily respected, as would be the case in a truly digital system. Therefore attention must be paid to meta-stability, gain, and other characteristics as for a comparator in an ADC. Some techniques to build a suitable flip-flop are discussed in [11]. However, for our design a flip-flop from a standard cell library is adequate. This digital approach does not rely on component matching or on any process dependant parameters such as inverter delays.

From a phase perspective, the PML incorporates an integrator in its feedback path. This is because the quantized phase information is fed back to the *frequency* control of the divider. As phase is the integral of frequency, this implies the presence of an integrator in the phase domain. Referring again to Fig. 3, the presence of this integrator changes nature of the transfer function from the VCO output ($\Phi_{\rm vco}$) to the output of the quantization flip-flop, and also changes the transfer function from the modulator input to the output of the flip-flop. A small-signal phase-domain model of the divider is shown in Fig. 4, the derivation of which is discussed in [12]. The phase transfer function from the VCO output to the output of the flip-flop is now high-pass instead of all-pass, because of the integrator in the feedback path. As shown in Fig. 3, a digital integrator placed at the output of the quantizer compensates for the change in transfer function that the PML has caused.

Fig. 5 shows an overview of the architecture with the proposed phase detector configuration. The output of the integrator goes to a DAC, which drives the analog control of the VCO, so as to complete the loop. $K_{\rm lp}$ is a digital gain that modifies the bandwidth of the outer loop, while gain block $K_{\rm pd}$ modifies the bandwidth of the inner loop.

A. Small-Signal Model

A small-signal model of the overall system is required in order to calculate the loop dynamics, and to predict the phase noise at the output. The overall approach for calculating phase noise is based on [12]. The general strategy is to begin with a linear model for each of the components. Using this, the closed-loop transfer function for the overall loop $G(f)$, is calculated. Next, the transfer function between each noise source and the PLL output is calculated using $G(f)$. In this way the phase noise at the output can be calculated in a straightforward manner. This is a linear analysis, and nonlinear effects within the loop are not considered.

The overall small-signal model for the system is shown in Fig. 6. The loops are labeled $G_1(f)$ and $G_2(f)$. The $\rm H_{lp}(f)$ term models an *RC* filter at the output of the DACs which filters the $\Sigma\Delta$ DAC's quantization noise. The overall model contains a mixture of discrete and continuous-time transfer functions and noise sources. The $K_{\rm fit}$ term is a fitting parameter that models the phase detector gain, as measured in simulation experiments. $N_{\rm nom}$ is the nominal division ratio, $K_{\rm vco}$ is the VCO gain, and $K_{\rm lp}$, $K_{\rm pd}$ are digital constants. The noise sources which are shown here are the phase detector quantizer noise ($\Phi_{\rm quant}[{\rm k}]$), the $\Sigma\Delta$ DAC noise ($\Phi_{\Sigma\Delta{\rm DAC}}[{\rm k}]$), the VCO phase noise (($\Phi_{\rm VCO}({\rm t})$), and the divider $\Sigma\Delta$ noise ($n_{\Sigma\Delta}[{\rm k}]$). In Fig. 6, sampling is denoted by the $1/{\rm T}$ transfer function, while the DAC is represented by the ${\rm T}$ block. This is because of the frequency domain relationship between a continuous time signal and its sampled equivalent, as described by $\hat{X}(f) = 1/T\sum_{k=-\infty}^{\infty} X(f-k/T)$. Deriving the loop transfer functions and the noise at the output involves approximating discrete noise sources as continuous ones, in a similar way to [12]. The analog transfer function for the PML is expressed in (1), where $A_1(f)$ is the open-loop gain:

$$G_1(f) = \frac{A_1(f)}{1 + A_1(f)}. \tag{1}$$

If the digital integrators are approximated as continuous time integrators of value $1/j2\pi fT$ then the open-loop gain can be given by

$$A_1(f) \cong \frac{K_{\rm fit}K_{\rm pd}}{N_{\rm nom}jfT}. \tag{2}$$

[1]In this work *Phase Minimization Loop* is preferred to *Frequency Discriminator*, as the feedback is used to minimize the *phase* difference at the input of the quantizer.

[2]Also [13]–[15] include analog integrators with charge pumps in order to implement higher order noise shaping of the frequency error, a step that has been avoided in this work in order to maximize the digital nature of the system.

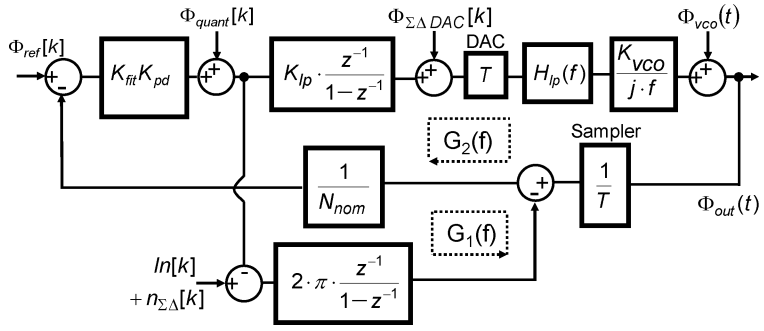

Fig. 6. Small-signal phase domain model will noise sources.

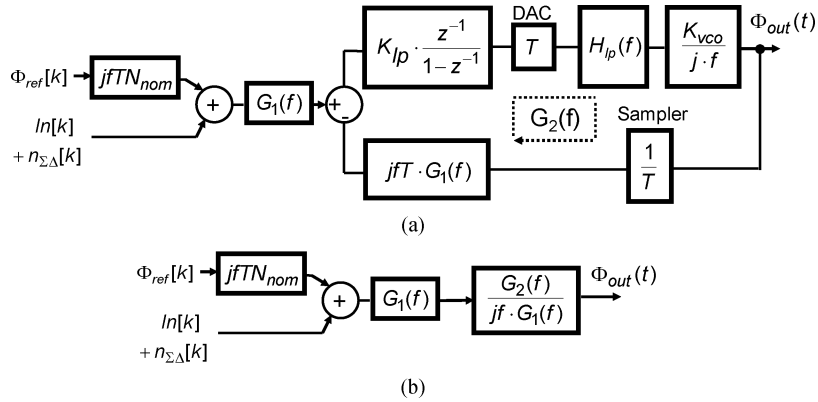

Fig. 7. (a) Simplified model for inner loop. (b) Simplified model for both loops.

Similarly, for the output loop, $G_2(f)$, the closed-loop and open-loop responses are given in (3) and (4), respectively:

$$G_2(f) = \frac{A_2(f)}{1 + A_2(f)} \tag{3}$$

$$A_2(f) \cong \frac{K_{\rm lp} K_{\rm vco} H_{\rm lp}(f) G_1(f)}{j2\pi f}. \tag{4}$$

If the higher order poles, $H_{\rm lp}(f)$, are ignored, then we can combine (1),(2),(3) and (4) to give the overall closed-loop response (5):

$$G_2(s) = \frac{\frac{2\pi}{TN_{\rm nom}} K_{\rm pd} K_{\rm vco} K_{\rm fit} K_{\rm lp}}{s^2 + s\frac{2\pi}{N_{\rm nom}T} K_{\rm fit} K_{\rm pd} + \frac{2\pi}{N_{\rm nom}T} K_{\rm pd} K_{\rm vco} K_{\rm fit} K_{\rm lp}}. \tag{5}$$

We note that this is an all pole system; there are no zeros. (Dual loop architectures have also been used in fiber optic communication PLLs to implement transfer function with no zeros [16].)

In Fig. 7(a) the loop is redrawn with the inner loop, $G_1(f)$, replaced with its equivalent transfer function. Here the only inputs considered are the reference, the frequency control word and $\Sigma\Delta$ noise. In Fig. 7(b) the outer loop, $G_2(f)$, is also replaced. From this it is straightforward to deduce the transfer functions from input to output. The relationship between the reference phase and output phase is given in (6). ($\Phi_{\rm ref}[{\rm k}]$ is first multiplied by T, to convert it to an approximate equivalent continuous time source.)

$$\frac{\phi_{out}(f)}{\phi_{\rm ref}[k] \cdot T} = \frac{1}{N_{\rm nom}} G_2(f) \tag{6}$$

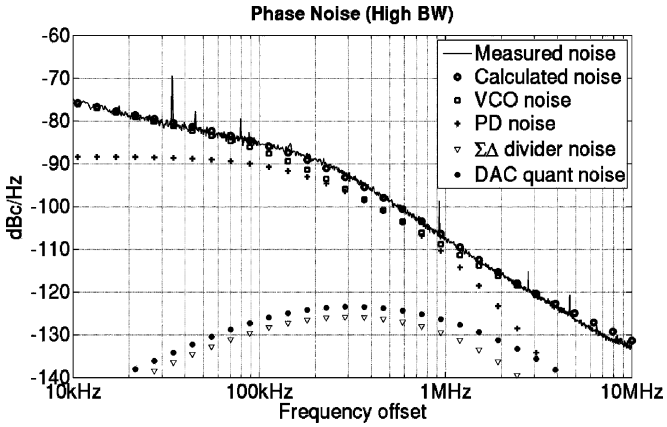

Fig. 8. Plot of measured and calculated noise sources.

In a similar manner, the transfer function for all of the noise sources can be calculated. The various noise sources, and the total calculated noise, and measured noise are plotted in Fig. 8. For low and very high frequencies the phase noise is dominated by the VCO noise, while for frequencies close to the loop bandwidth (142 kHz) the phase detector quantization noise (PD noise in Fig. 8) is significant. The poor VCO phase noise performance is due in part to the low quality factor of available integrated inductors on this process. The divider $\Sigma\Delta$ noise does not make a significant contribution to the output phase noise. This is because the reference clock used is large in comparison to the loop bandwidth, and hence most of the $\Sigma\Delta$ quantization noise is shaped to outside of the PLL loop bandwidth.

Both of the two PLL loops contain a single net integrator, and therefore each loop is a Type 1 loop. This may seem surprising

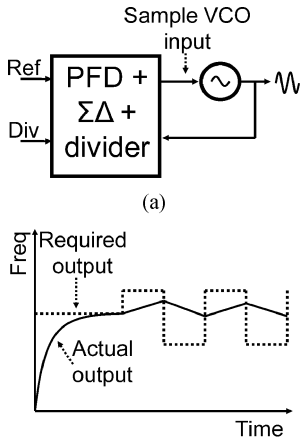

Fig. 9. (a) Simplified PLL. Input to VCO is analogous to the output frequency. (b) Plot of required output versus actual output.

considering that the small-signal diagram of Fig. 6 appears to incorporate two integrators in the outer loop ($G_2(f)$); the VCO and the digital integrator at the output of the phase quantizer. However as already mentioned, the digital integrator cancels the zero introduced by the PML, leaving a *net* single DC pole.

III. Sampling Scheme

The wide fractional-N PLL loop-bandwidth required for high-speed modulation, conflicts with the low loop bandwidth favored for suppression of $\Sigma\Delta$ noise, phase detector noise, and reference jitter. In this section, a new technique which breaks the link between loop-bandwidth and the modulation rate for frequency-shift-keying schemes is presented. In a standard FPLL, the output frequency is modified by changing the division ratio control, eventually leading to a change in the VCO control voltage. If the exact VCO gain were known, then in addition to changing the division ratio control, a signal could be injected directly into the input of the VCO, as in two point modulation. In the proposed scheme, knowledge of the exact VCO gain is not required. Instead, using some simple signal processing, the required step size at the input of VCO is learned from previous changes in VCO control in response to changes in the modulator input.[3]

Consider the case where the loop is to switch between two output different frequencies, A and B, such as for 2-FSK, and assume that the loop frequency is initially settled at the average of A and B. If the bandwidth of the loop is not large enough in a standard FPLL then the frequency never settles correctly to A or B [Fig. 9(b)]. In Fig. 9(a) a simplified version of the PLL is shown. The input to the VCO can be considered to be analogous to the frequency of the output signal, and it follows that if the output frequency is to switch instantaneously then the input to VCO must also switch instantaneously. In the proposed scheme at the end of each data-bit period the digital value that determines the VCO input is sampled. When switching between the two desired frequencies, A and B, the most recently sampled values are subtracted from each other. The result of this subtraction ["*Delta*" in Fig. 10(a)] is added to the VCO control

[3]In summary, this is a form of two point modulation with a simple calibration scheme.

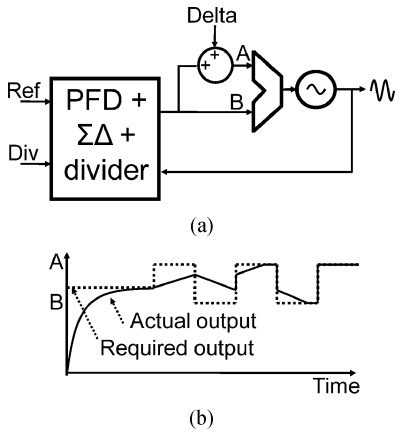

Fig. 10. (a) PLL with Delta added. (b) Simulation VCO input.

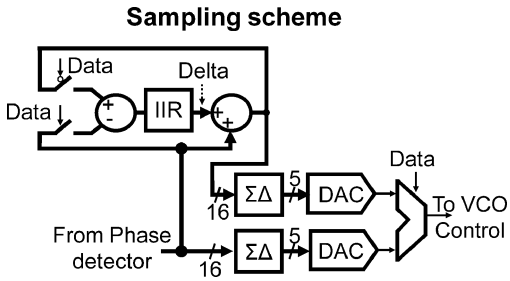

Fig. 11. Details of the sampling scheme.

for frequency A, to give an initial digital VCO control value for frequency B. As the required frequency continues to switch between frequencies A and B, then the sampled value of *Delta* converges on the correct VCO input difference for the required frequencies A and B. In other words, the sampling scheme iteratively learns the required step size *Delta*. Fig. 10(b) shows the output frequency, using the sampling scheme. As can be seen, after a few iterations *Delta* reaches the correct step size, and the frequency is able to switch instantaneously. The loop bandwidth determines how quickly Delta reaches its final value, but does not affect the switching frequency. This does not presuppose any knowledge of the analog characteristics of the loop, aside from monotonic behavior. For example if the VCO gain were to change due supply or temperature changes then the value of *Delta* would be quickly updated. This scheme does not update every reference period; *Delta* is only updated on the edges of the data to be transmitted. A disadvantage of this approach is its lack of generality; that is it can only be used for modulation schemes which are limited to a small set of discrete frequencies, such as unfiltered 2-FSK.

A more detailed block diagram of the sampling scheme is shown in Fig. 11. The control path for the VCO is split into two paths, one path for each of the two frequencies A and B. Each path contains a $\Sigma\Delta$ DAC, the output of which goes to an analog multiplexer. The two DAC control signals are sampled when the transmission data transitions from zero to one and from one to zero, which corresponds to the switching instants from frequency A to B and from frequency B to A, respectively. The difference, *Delta*, is then added to the signal from the phase detector. Multiplexing between the two DACs is done in the

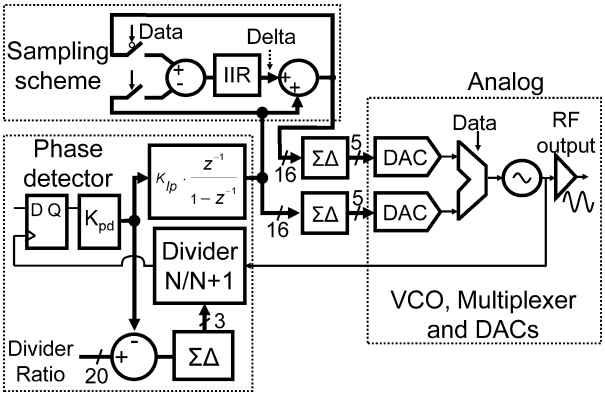

Fig. 12. Complete architecture.

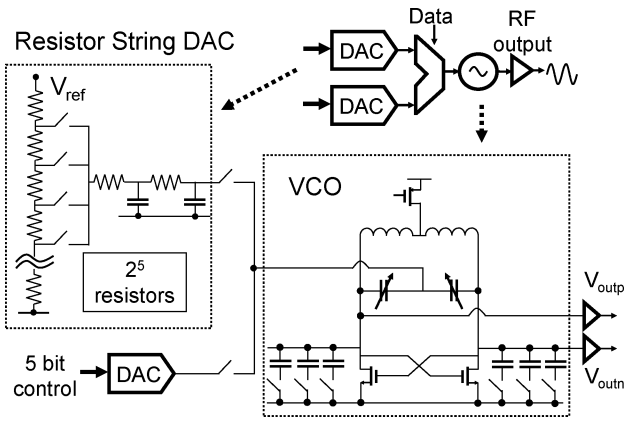

Fig. 13. Overview of analog section.

analog domain after the reconstruction filters. The filters contain two higher order RC poles to filter the DAC $\Sigma\Delta$ noise. As the input to the VCO is required to change instantaneously, the multiplexer must be placed after these poles.

The complete architecture including the digital phase detector and the new sampling scheme is shown in Fig. 12. The frequency switching method allows fast frequency modulation within a low loop bandwidth, as the frequency switching is not limited by the bandwidth of the loop, provided that the loop needs only to switch between a small number of discrete frequencies. This also demonstrates the usefulness of having all the relevant signals in the digital domain. An analog equivalent of the above scheme is possible in principle, however implementing the samplers, adders and subtractors as analog circuits would introduce debilitating additional complexity.

IV. Implementation Details

A reference clock of 185.5 MHz is used, with a nominal output frequency 2.24 GHz, which corresponds to a nominal division ratio of $N_{\rm nom} = 12.075$. $K_{\rm pd}$ was set to 0.01, and the loop gain ($K_{\rm lp}$) is set at 0.025, resulting in a loop bandwidth of 142 kHz. The PML loop has an estimated bandwidth of 1.2 MHz. The VCO analog gain is 25 MHz/V, and an additional 500 MHz tuning range is achieved using digital switches which add or remove VCO capacitance. From simulation experiments, the acquisition range was determined to be approximately $\pm$150 MHz, which is significantly larger that the VCO tuning range, and so no additional acquisition aids were implemented. The analog tuning range is deliberately made small in order to prevent DAC quantization noise from excessively contributing to the output phase noise. A relatively high reference frequency is required, so that the phase quantizer is adequately oversampled. Each doubling of the oversampling rate leads to a 3 dB reduction in in-band quantization noise.

In order to convert from the digital to the analog domain, a first order $\Sigma\Delta$ controls a simple 5 bit string DAC. If a higher frequency reference clock or a DAC quantizer with more bits is used, then the VCO analog tuning range can be increased without degrading output phase noise. An alterative approach would be to implement a fully digitally controlled oscillator, such as presented in [17]. The programmable divider is based on the modular architecture presented in [18], where each of the 2/3 divider cells is identical. The divider division ratio can be set from 8 to 15. An overview of the DAC and VCO is shown in Fig. 13. Each DAC draws 1.4 mA from the 1.4 V supply, and the VCO draws approximately 2 mA. The digital auto-route, which includes all of digital except the divider, consumes approximately 6 mW.

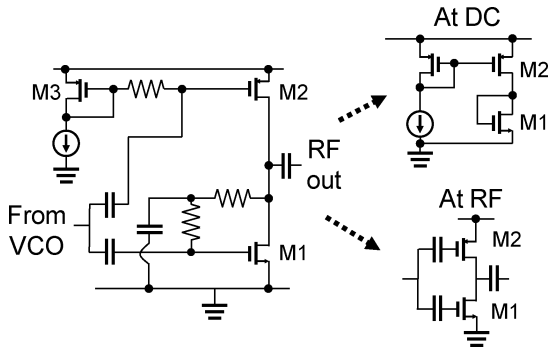

Fig. 14. Output buffer.

The design of even simple output buffers in very low headroom processes is not trivial. If a source follower were used, then enough headroom would be required for both the signal swing and the $\rm V_t$ of the MOS devices. In this work a simple output buffer is used, which requires little headroom, and sets the DC value of the output node automatically, without requiring complex common mode feedback circuitry. The buffer is shown in Fig. 14. At DC, the buffer acts a current source driving current into a diode connected load. In this way the DC point of the output will be approximately $\rm V_{dc} = V_{dsat} + V_t$, which will be close to $\rm V_{dd}/2$ for this process. On the other hand, at high frequencies, the buffer acts as a push-pull amplifier. The DC values at the input and output of the buffer are not important, as both input and output are ac coupled.

The prototype transmitter is implemented in 0.13 μm mixed-mode CMOS and occupies an active area of 0.7 mm^2, and a total area of 2 mm^2 including pads. The layout of the prototype is shown in Fig. 15. It is worth noting that even though many of the analog components have been removed, the area is still dominated by the area of the remaining analog blocks. The digital auto-routed logic takes up 0.075 mm^2, a small fraction of the overall area, despite dominating the architecture shown in

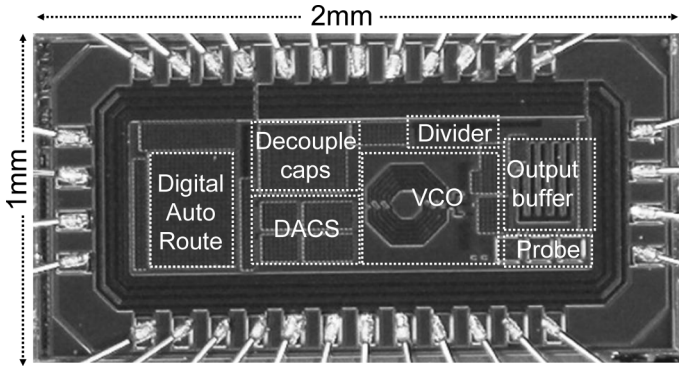

Fig. 15. Micrograph.

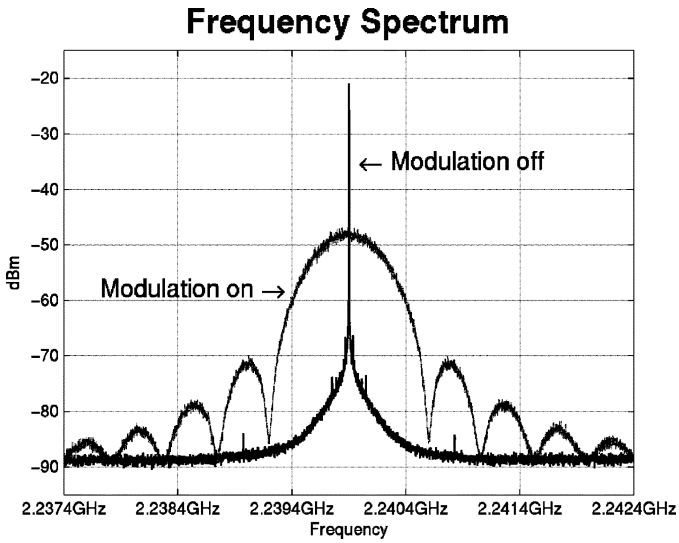

Fig. 16. Modulation spectrum.

Fig. 12. This demonstrates the area savings that can be achieved by going from an analog dominated architecture to a digital dominated architecture.

V. Results and Conclusion

The prototype consumes 14 mW from a 1.4 V supply. Fig. 16 shows the measured output spectrums for a pure synthesized tone and for random data with an FSK data modulation rate of 927.5 kbits/s. Fig. 8 shows the measured phase noise.

The VCO was originally intended to operate in the 2.4 GHz ISM band. However, due to process variation, the maximum VCO frequency was 2.24 GHz, even considering the digital tuning capacitors. Fig. 17 shows a trellis diagram of the measured output phase. In this measurement various random data patterns are applied to the FPLL, and the corresponding phase change at the output is measured, and overlaid. As can be seen, the phase changes direction instantaneously, which is the equivalent to the frequency changing instantaneously. Even with a loop bandwidth of 142 kHz, a data rate of 927.5 kb/s is still possible. Without the new switching scheme the data rate would be restricted to a fraction of the loop bandwidth.

In this work, two techniques are proposed and demonstrated. First, a digital phase detector allows a significant portion of the analog circuitry required in a FPLL to be replaced with digital

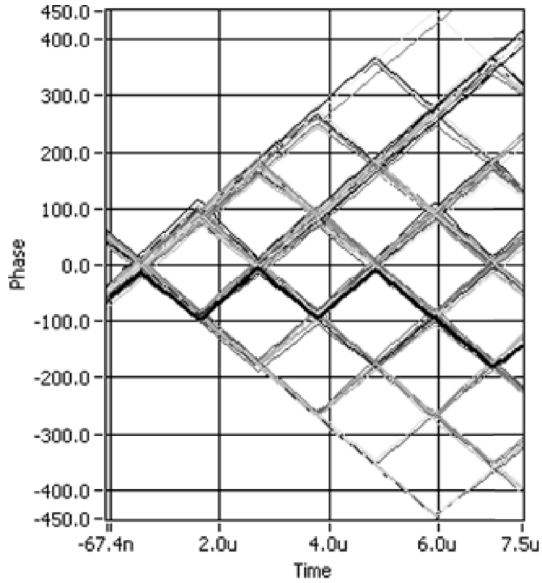

Fig. 17. Trellis diagram of phase output.

equivalents. In addition, a new technique has been developed which allows for frequency modulation at a rate significantly faster rate than the loop bandwidth. As transistor gate length continues to scale down, design of analog circuitry will become even more challenging, while the area and power costs of digital circuits continues to decrease. Techniques such as the ones presented here will become crucial in order to move from analog dominated circuitry to digital circuitry.

Acknowledgment

The authors acknowledge the support of Intel. They would also like to thank all of the people who provided invaluable advice and support throughout this project, including J. Kang, J.-Y. Chen, M. Mansuri, S. Naraghi, J. Pernillo, I. Bogue, D. Shi, F. Kocer, and C. Conroy. Architectural investigation was aided by CppSim [19]. The authors also thank the reviewers for invaluable insights and suggestions.

References

[1] T. A. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[2] E. Gotz, H. Krobel, G. Marzinger, B. Memmler, C. Munker, B. Neurauter, D. Romer, J. Rubach, W. Schelmbauer, M. Scholz, M. Simon, U. Steinacker, and C. Stoger, "A quad-band low power single chip direct conversion CMOS transceiver with $\Sigma\Delta$-modulation loop for GSM," in *Proc. Eur. Solid-State Circuits Conf.*, 2003, pp. 217–220.

[3] I. Galton, "Delta-sigma data conversion in wireless transceivers," *IEEE Trans. Theory Tech.*, vol. 50, no. 1, pp. 302–315, Jan. 2002.

[4] M. H. Perrott, "Techniques for high data rate modulation and low power operation of fractional-N frequency synthesizers," Ph.D. dissertation, Massachusetts Inst. Technol. (MIT), Cambridge, MA, 1997.

[5] R. A. Meyers and P. H. Waters, "Synthesizer review for pan-European digital cellular radio," in *Proc. IEEE VLSI Implementations for Second Generation Digital Cordless and Mobile Telecommunication Systems Colloq.*, 1990, pp. 8/1–8/8.

[6] M. Gupta and B. Song, "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2842–2851, Dec. 2006.

[7] A. Swaminathan, K. Wang, and I. Galton, "A wide-bandwidth 2.4 GHz ISM band fractional-N PLL with adaptive phase noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, Dec. 2007.

[8] R. Staszewski, J. Wallberg, C. M. Hung, G. Feygin, M. Entezari, and D. Leipold, "LMS-based calibration of an RF digitally controlled oscillator for mobile phones," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 3, pp. 225–229, Mar. 2006.

[9] M. Ferriss and M. P. Flynn, "A 14 mW fractional-N PLL modulator with an enhanced digital phase detector and frequency switching scheme," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 353–353.

[10] R. C. Walker, "Designing bang-bang PLLs for clock and data recovery in serial data transmission systems," in *Phase-Locking in High-Performance Systems*. Piscataway, NJ: IEEE Press, 2003.

[11] R. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 3, pp. 220–224, Mar. 2006.

[12] M. H. Perrott and M. D. Trott, "A modeling approach for Σ-Δ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug. 2002.

[13] R. Beards and M. Copeland, "An oversampling delta-sigma frequency discriminator," *IEEE Trans. Circuits Syst. II*, vol. 41, no. 1, pp. 26–32, Jan. 1994.

[14] W. Bax, T. Riley, C. Plett, and M. Copeland, "A $\Sigma\Delta$ frequency discriminator based synthesizer," in *Proc. Int. Symp. Circuits and Systems (ISCAS)*, 1995, pp. 1–4.

[15] W. Bax and M. Copeland, "A GMSK modulator using $\Sigma\Delta$ frequency discriminator-based synthesizer," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1218–1227, Aug. 2001.

[16] T. H. Lee and J. F. Bulzacchelli, "A 155-MHz clock recovery delay- and phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1736–1746, Dec. 1992.

[17] C. M. Hung, R. B. Staszewski, N. Barton, M. C. Lee, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.

[18] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000.

[19] M. H. Perrott, CppSim Behavioral Simulator Package. [Online]. Available: http://www-mtl.mit.edu/researchgroups/perrottgroup/tools.html

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