A 4-GS/s 4-bit Flash ADC in 0.18-μm CMOS

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***Abstract*—A 4-bit noninterleaved flash ADC implemented in 0.18-μm digital CMOS achieves a sampling rate of 4 GS/s. A 32 μm by 32 μm, on-chip differential inductor in each comparator extends the sampling rate without an increase in power consumption. A combination of DAC trimming and comparator redundancy reduces the measured DNL and INL to less than 0.15 LSB and 0.24 LSB, respectively. The measured ENOB with a 100 MHz full-power input is 3.84 bits and 3.48 bits, at 3 GS/s and 4 GS/s, respectively. The ADC achieves a bit error rate of less than 10^{-11} at 4 GS/s.**

***Index Terms*—CMOS, comparator, comparator redundancy, DAC trimming, flash analog-to-digital converter, metastability, monolithic inductor, offset correction, regenerative time constant.**

I. Introduction

HIGH-SPEED, low-resolution analog-to-digital converters (ADCs) are used in data storage read channels [1], [2], in broadband wired and wireless communication systems [3]–[9], in digital oscilloscopes [10]–[12], and in regulators [13]. Although the maximum sampling rate of an ADC can be extended by using a process that offers faster devices (e.g., GaAs [10]), or by time-interleaving ADCs [3], [9], [11], [12], [14]–[16], circuit techniques that extend the sampling rate, for a given CMOS technology, are still fundamentally required. The flash ADC architecture [17] generally achieves the highest sampling rate, and comparator performance typically determines maximum sampling speed. A comparator's sampling speed is mostly determined by its regeneration time constant, and the regeneration time constant is inversely proportional to the square of the gate length for a given CMOS technology [18]. We present a flash ADC architecture, implemented in digital 0.18-μm CMOS, that achieves up to 4 GS/s with a low measured rate of the metastability [19]. High sampling speed is made possible through the addition of inductors in the regenerative comparator core and through the use of small, fast transistors. The large mismatches and offsets caused by the small transistors are cancelled out by a combination of trimming and comparator redundancy. Redundancy relaxes the required resolution of the trim DAC.

We review the operation of regenerative comparators and present the new techniques that are applied to the comparator core in Section II. The benefits of the addition of the inductors are quantified and practical aspects of the implementation, in particular the size of the inductors, are discussed. The addition of inductors has a different effect on the tracking, reset and latching phases: therefore, the choice of inductance value to achieve the best overall performance is also discussed. In Section III, we present the entire comparator, including the comparator core. In Section IV, we discuss DAC trimming and redundancy. The benefit of using both techniques together is analyzed from a yield perspective. The overall ADC architecture is described in Section V, and the measurement results are given in Section VI.

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II. Comparator Core

A. Review

The differential output $\mathrm{V_{out}}$ of the comparator core, shown as a single-ended input version in Fig. 1 (for simplicity), is decided based on the polarity of the difference between the analog input $\mathrm{V_{in}}$ and the reference $\mathrm{V_{ref}}$. When the differential clock inputs $\mathrm{V_{clkm}}$ and $\mathrm{V_{clkp}}$ are high and low respectively, the comparator core operates in the *tracking phase* [Fig. 2(a)]. During this phase, the cross-coupled devices are disabled, and $\mathrm{V_{out}}$ tracks the difference between $\mathrm{V_{in}}$ and $\mathrm{V_{ref}}$ with the pre-amplification voltage gain. When clock $\mathrm{V_{clkp}}$ is high, the comparator core operates in the *regenerative phase* [Fig. 2(b)]. During regeneration, the input pair is disabled and the cross-coupled devices produce a large regenerative voltage gain. When $\mathrm{V_{clkm}}$ returns high, the *latched* memory is removed and the tracking phase begins for the next sample.

During the tracking phase, $\mathrm{V_{out}}$ is given by

$$\mathrm{V_{out}} = \mathrm{V}_r \cdot \exp(-t/\tau_t) + G_t \cdot (\mathrm{V_{in}} - \mathrm{V_{ref}}) \cdot \{1 - \exp(-t/\tau_t)\} \tag{1}$$

where V_r is the latched output from the previous regenerative phase, τ_t is the tracking mode time constant of the comparator core, and G_t is the tracking gain. For an output parasitic capacitance C and load resistance R, τ_t is given by

$$\tau_t = R \cdot C. \tag{2}$$

At the beginning of the regenerative phase, $\mathrm{V_{out}}$ is given by

$$\mathrm{V_{out}} = \mathrm{V}_t \cdot \exp(t/\tau_r) \tag{3}$$

where V_t is the final output at the end of the tracking phase (or at the beginning of the regeneration), and τ_r is the regeneration mode time constant. If the transconductance of the cross-coupled devices is g_m, then τ_r is given by

$$\tau_r = \frac{C}{g_m - 1/R}. \tag{4}$$

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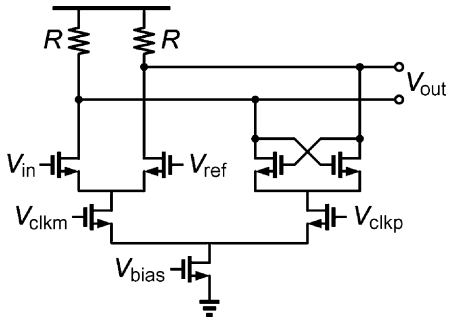

Fig. 1. Comparator core.

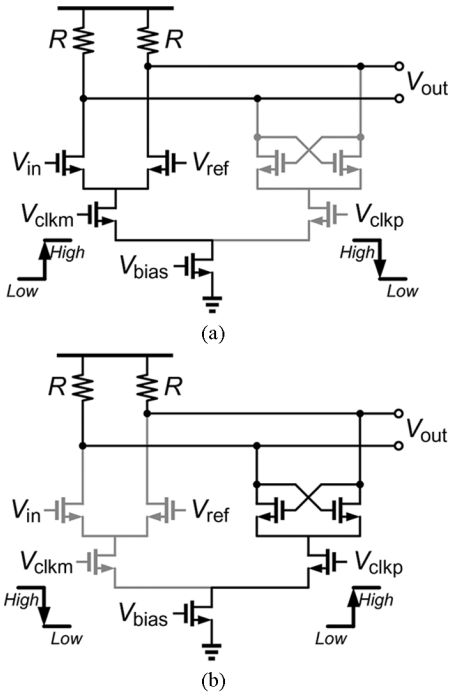

Fig. 2. Operation of the comparator core. (a) Tracking phase. (b) Regenerative phase.

B. Comparator Core With Inductors

The regeneration mode time constant τ_r and the tracking mode time constant τ_t are reduced by placing inductors in series with the load resistors (Fig. 3), thereby increasing the maximum sampling speed for a given power consumption. The tracking mode time constant τ_t is reduced through inductive peaking, as in a linear amplifier.[1] We explain the reduction in the regeneration mode time constant τ_r, by considering the load incorporating an inductor as an equivalent *RC* load. Fig. 4 shows the transformation, with Fig. 4(a) showing the comparator output load with R, C, and L, and Fig. 4(b) shows the equivalent load with R_{eff} and C_{eff}.[2] R_{eff} and C_{eff}, at a frequency ω, are given by

$$R_{\text{eff}} = R + \frac{\omega^2 L^2}{R} \tag{5}$$

[1]Inductive peaking is also known as shunt peaking. This technique was first used to increase the bandwidth of vacuum tube based amplifiers, used in televisions, in the 1930s [20].

[2]Ref. [21] shows that this one-pole approximation holds as long as $g_m \cdot R > 1$ holds. This inequality is a necessary condition for latching.

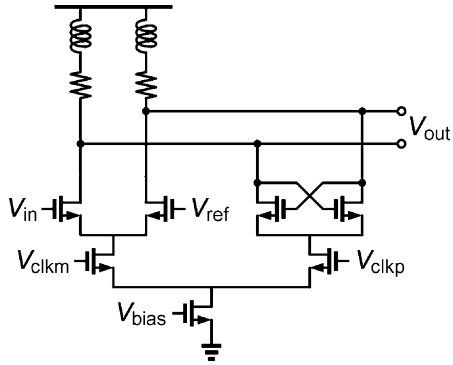

Fig. 3. Comparator core with inductors.

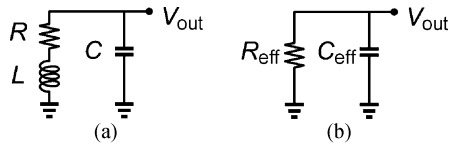

Fig. 4. Concept of effective resistance and capacitance. (a) Output load. (b) Equivalent output *RC* load.

and

$$C_{\text{eff}} = C - \frac{L}{R^2 + \omega^2 L^2}. \tag{6}$$

The new regeneration mode time constant τ_{r_L} is given by

$$\tau_{r\_L} = \frac{C_{\text{eff}}}{g_m - 1/R_{\text{eff}}}. \tag{7}$$

We note that R_{eff} is always greater than R, and C_{eff} is always smaller than C. Therefore, for a nonzero inductance, we see that τ_{r_L} is always smaller than τ_t.

We now discuss the optimum selection of inductance. As discussed above, a nonzero inductance improves the regeneration speed, and a more detailed analysis [21] shows that the regenerative time constant τ_{r_L} decreases monotonically with L. Therefore, the largest possible inductance is preferred.[3] On the other hand, however, during the reset phase (i.e., at the beginning of the next sample), the inductance should not be so large that it causes ringing, since under-damped settling slows reset. This limitation sets a maximum value of inductance that corresponds to critical damping ($L = R^2C/2.41$ [20]). Finally, setting $L = R^2C/1.41$ [20], leads to the maximum tracking bandwidth.

To achieve optimum performance, the behavior during the reset, tracking and regenerative phases should be considered. The regeneration mode time constant (τ_{r_L}) with an inductance L is given by [21]

$$\tau_{r\_L} = \frac{2}{\left(\frac{g_m}{C} - \frac{R}{L}\right) + \sqrt{\left(\frac{g_m}{C} - \frac{R}{L}\right)^2 + 4\left(\frac{g_m R - 1}{LC}\right)}}. \tag{8}$$

The tracking time constant (τ_{t_L}) with an inductance L is given by [20]

$$\tau_{t\_L} = \frac{RC}{\sqrt{\left(\frac{-m^2}{2} + m + 1\right) + \sqrt{\left(\frac{-m^2}{2} + m + 1\right) + m^2}}} \tag{9}$$

[3]Oscillation is unlikely because of the large load resistance.

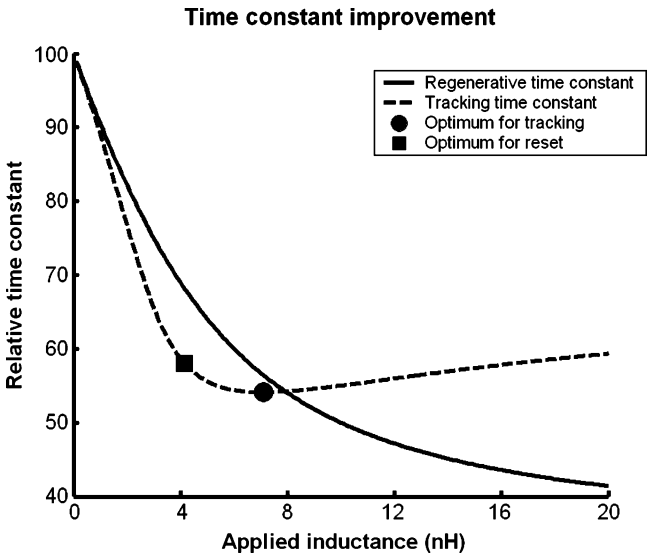

Fig. 5. Tracking and regeneration mode time constants versus applied inductance.

with

$$m = R^2C/L. \tag{10}$$

Fig. 5 shows τ_{r_L} and τ_{t_L} versus applied inductance. The figure is based on (8)–(10), and we use regeneration mode transconductance $g_m = 3$ mA/V, $R = 500\ \Omega$, and $C = 40$ fF. The figure also shows optimum inductances for reset and tracking. Practical optimization of the inductance for the prototype ADC was achieved with the help of the *overdrive test* [22].

We can significantly reduce the area required for the inductors by considering the parasitic series resistance of the inductors as a part of the total load resistance. Since the inductors can now have a large resistive loss, we can use a narrow metal trace to implement them in a small area [23].[4] We use a stacked inductor comprised of metal layers M2 and M5 in series to further reduce the inductor area for a given inductance. This choice of the metal layers gives the maximum self-resonant frequency (12 GHz). Furthermore, we use a differential inductor structure instead of a pair of separate inductors. A differential inductor structure generates strong magnetic coupling between the two inductors, further reducing the overall area to achieve a given inductance. The resulting 11.88 nH, 10 turn, 0.4 μm metal trace differential inductor occupies an area of 32 μm by 32 μm. With a 32 μm separation between inductors in adjacent comparators, the magnetic coupling coefficient is less than 0.005 [24]. With such small coupling, there is little effect on the inductors of adjacent comparators. Each differential inductor has a parasitic resistance of 406 Ω.

Fig. 6 shows a full schematic of the comparator core. $\mathrm{V_{ip}}$ and $\mathrm{V_{im}}$ are the differential analog inputs, and $\mathrm{V_{rp}}$ and $\mathrm{V_{rm}}$ are the differential references. $\mathrm{V_{clkp}}$ and $\mathrm{V_{clkm}}$ are the complementary clocks. The cascode devices $(\mathrm{M_{1,2}})$ reduce the parasitic capacitance presented at the load and also reduce kickback noise. Thanks to the cascode devices, two transistor drains ($\mathrm{M_{1,2}}$ and $\mathrm{M_{7,8}}$), not three, are connected to each load resistor (i.e., without the cascode devices, two of the *differential* input transistors and the one of the cross-coupled transistors would connect to each load). Thanks to the reduced parasitic capacitance, the comparator has a larger bandwidth during the *tracking* phase, and a smaller regeneration mode time constant during the *regeneration* phase. The cascode devices also reduce the kickback noise from the comparator to the input during the reset phase. The differential current sources $(\mathrm{M_{13,14}})$ improve the input and reference common mode rejection. A drain current of 500 μA flows through $\mathrm{M_{13}}$ and $\mathrm{M_{14}}$.

[4]In [23], the inductor parasitic resistance is used as part of the load resistance in an inductively peaked amplifier.

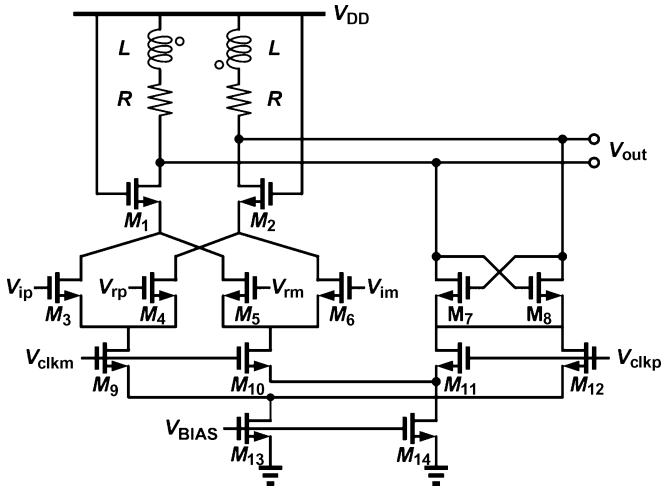

Fig. 6. Comparator core.

III. Other Comparator Stages

Fig. 7 shows the entire comparator. The comparator core is discussed in Section II. The second and third stages (shown in Fig. 8) are identical latches [7], operating on alternate clock edges. These pipelined latches provide additional voltage gain, generating rail-to-rail signals and reducing the probability of metastability. A D-type flip-flop (D-FF, shown in Fig. 9) stores the comparator output so that the encoder can reliably perform thermometer-code to binary-code conversion. The back-to-back inverter structure of the D-FF [25] provides additional regeneration, further reducing the probability of a metastable digital output. This static D-FF reliably works not only at 4 GHz, but also at very low clock frequencies. Fig. 10 shows a timing diagram of the entire comparator.

IV. Offset Calibration

Comparator offset is predominantly caused by transistor mismatches, and especially by MOS transistor threshold-voltage mismatches and by MOS transistor current-factor mismatches [26]. As we increase ADC sampling rate, input-referred comparator offset tends to increase, because minimum gate length devices are used to minimize parasitic capacitance, and because the tracking (or pre-amplification) gain is reduced to achieve a larger tracking bandwidth. When referred to the input, offsets caused by mismatches in the latching devices are divided by the tracking gain, and this input-referred offset increases

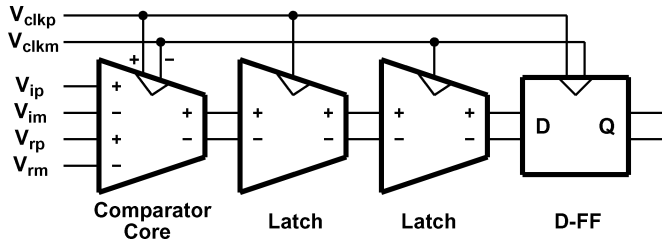

Fig. 7. Entire comparator.

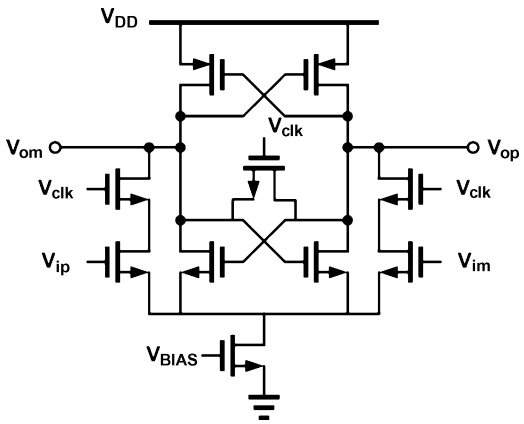

Fig. 8. Latch [7].

as the tracking gain is reduced. We use a combination of current-DAC-controlled trimming and comparator redundancy, to allow fast, small, efficient transistors to be used, and at the same time to achieve small measured values of INL and DNL. A trim current from a current DAC is applied to the comparator core. One redundant comparator is added for each ADC code, significantly relaxing the required trim DAC range and resolution.

A. Operation

Fig. 11 explains the current-trimming and comparator redundancy. A differential programmable current ($I_{\mathrm{DAC\_p}}$, $I_{\mathrm{DAC\_m}}$) is injected into the comparator core by a current-output digital-to-analog converter (DAC) to minimize the input-referred comparator offset. The cascode devices M_c separate the DAC output capacitance from the comparator core. During calibration, both the differential input ($\mathrm{V_{ip}} - \mathrm{V_{im}}$ in Fig. 6) and the differential reference input ($\mathrm{V_{rp}} - \mathrm{V_{rm}}$ in Fig. 6) are set to zero, so that the digital output of the comparator is determined only by the comparator offset.

The DAC current is initially completely steered in one direction to deliberately generate a large initial offset. The DAC current is incremented in 1-LSB DAC steps in the other direction until either the comparator output changes polarity or the DAC current is completely steered in the other direction. Since this DAC search is based on the overall comparator digital output (i.e., the output of the D-FF following the comparator), this scheme corrects the offsets of both the comparator core and the following latches. During calibration, the DAC clock is 256 times slower than the comparator sampling clock to provide sufficient settling time for the DAC output. This current-trimming scheme corrects the comparator offsets up to ± 0.64 LSB with an accuracy of 0.08 LSB. The DAC LSB size is 4 μA.

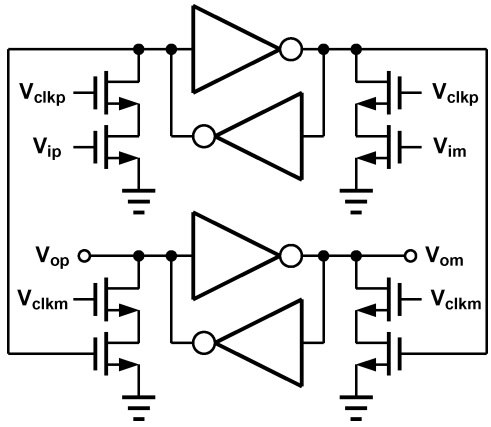

Fig. 9. D-FF schematic [25].

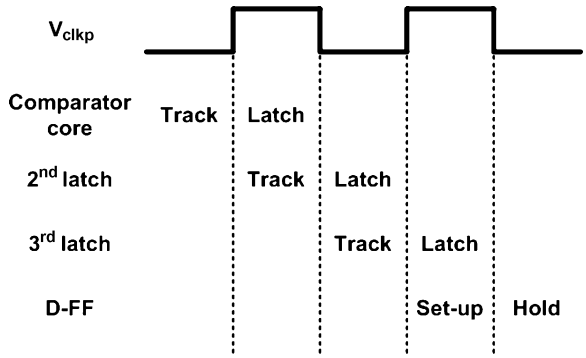

Fig. 10. Timing diagram of the entire comparator.

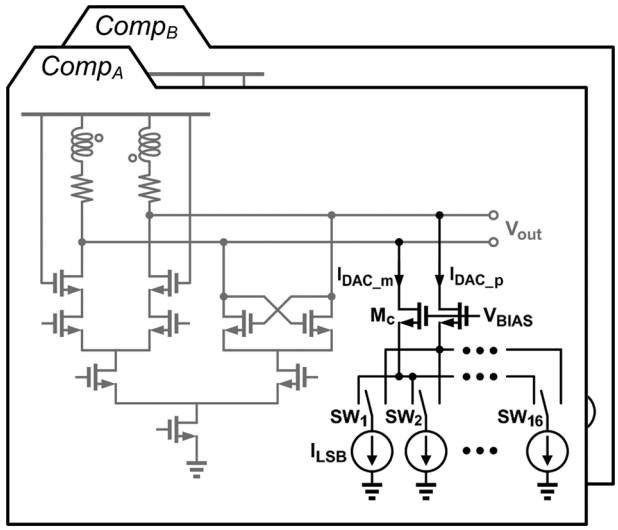

Fig. 11. Current trimming by a DAC and comparator redundancy.

In the prototype ADC, there are two comparator candidates for each ADC trip point: $Comp_A$ and redundant comparator $Comp_B$.[5] We select $Comp_B$ instead of $Comp_A$ if $Comp_A$ has an offset that is too large to be corrected by its trim DAC. $Comp_A$ is deemed to be uncorrectable if the differential current of its trim DAC is steered completely in one direction during

[5]Instead of redundant comparators, redundant load resistors or redundant input pairs can be used to save area.

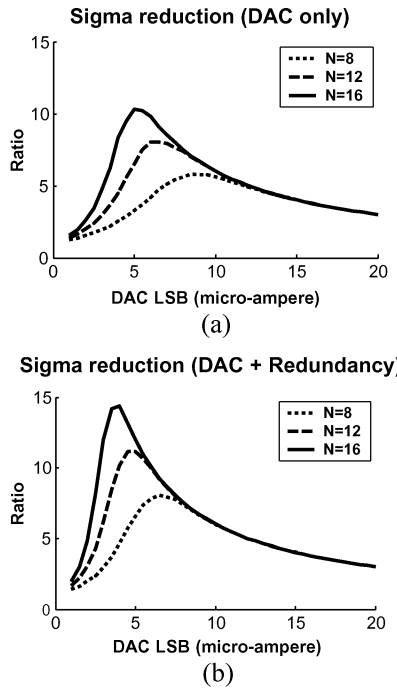

Fig. 12. Reduction ratio comparing uncalibrated with calibrated comparator offset standard deviation. (a) With DAC trimming. (b) With DAC trimming and comparator redundancy.

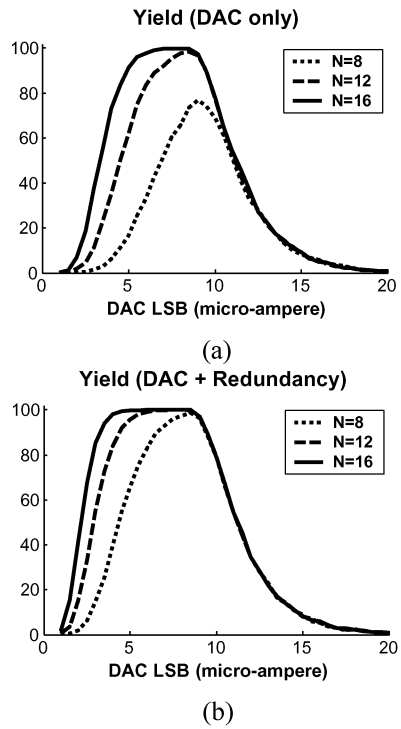

Fig. 13. ADC yield. (a) With DAC trimming. (b) With DAC trimming and comparator redundancy.

calibration without change in the digital output. After calibration, we simply turn off the unselected comparators to save power consumption. We note that this calibration scheme corrects both static and dynamic offsets of the comparator, since we use the same sampling clock frequency for the comparator during calibration and normal operations. In the prototype ADC, the calibration logic is implemented entirely on-chip and only a start signal is required to initiate calibration. Calibration takes 2.048 μs at 4 GS/s.

B. Optimization of Trim DAC Range and LSB Size

We now show how we optimize the DAC parameters (resolution and LSB size), and how redundancy helps to further suppress comparator offset and improve the yield of ADC (or to reduce DAC complexity). Initially, we assume that the threshold voltage mismatch and the current factor mismatch dominate the overall comparator offset. Fig. 12 shows Monte Carlo simulation results showing how much offset reduction we achieve after calibration, in terms of the standard deviation of the comparator offset, with various DAC LSB current sizes $(I_{\rm LSB})$ and DAC resolutions (N codes) ranging from 8 to 16 codes. Fig. 12(a) shows the ratio of uncalibrated to calibrated offset standard deviation versus $I_{\rm LSB}$ with DAC trimming only, while Fig. 12(b) shows the offset reduction ratio versus $I_{\rm LSB}$ when both DAC trimming and comparator redundancy are employed (with two comparator candidates per ADC code).

We see that there is an optimal value of $I_{\rm LSB}$ for each value of N. For a given N, we have limited trimming accuracy when $I_{\rm LSB}$ is too large. On the other hand, however, we have limited offset coverage range when $I_{\rm LSB}$ is too small. We achieve more offset reduction when there are redundant comparators, for a given N and $I_{\rm LSB}$. (This is because the probability of having two comparators with large offsets is much smaller than that of having a single comparator with a large offset.) In other words, the comparator redundancy reduces trim DAC complexity for a given trimmed offset sigma goal (and yield goal). As an example, we achieve a better offset reduction ratio when we use both comparator redundancy and DAC trimming with $N = 12$ (ratio $= 11.2$ when $I_{\rm LSB} = 5$ μA) compared to when we use the DAC trimming alone with $N = 16$ (ratio $= 10.3$ when $I_{\rm LSB} = 5$ μA).

Fig. 13 shows ADC yield versus $I_{\rm LSB}$ for various resolutions (N) ranging from 8 to 16 codes. For this yield simulation, we define a good ADC as having a maximum DNL between -0.2 LSB and 0.2 LSB. Fig. 13(a) shows the ADC yield when we apply the DAC trimming only and Fig. 13(b) shows the ADC yield when we apply both the DAC trimming and the comparator redundancy. We see that comparator redundancy also improves the ADC yield for a given $I_{\rm LSB}$ and N. In other words, we achieve a similar yield with reduced DAC complexity. For example, to achieve a yield over 98%, $N = 8$ is enough with the DAC trimming and the comparator redundancy together, while we need $N = 12$ with the DAC trimming alone. In the prototype, we use $N = 16$ and $I_{\rm LSB} = 4$–5 μA to maximize the offset reduction and the ADC yield.[6]

V. ADC Architecture

Fig. 14 shows the overall ADC architecture. The analog input $V_{\rm in}$ is directly fed to the 15 comparator sets. A track-and-hold

[6]We use $I_{\rm LSB} = 4$ μA in the data of the measurement section. We notice little difference when we use $I_{\rm LSB} = 5$ μA.

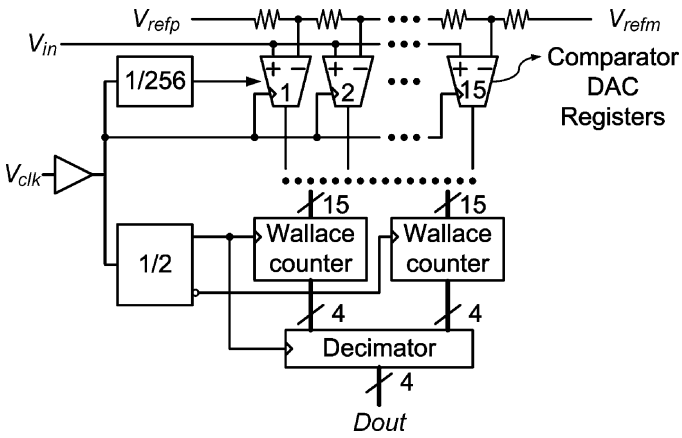

Fig. 14. Architecture of the ADC.

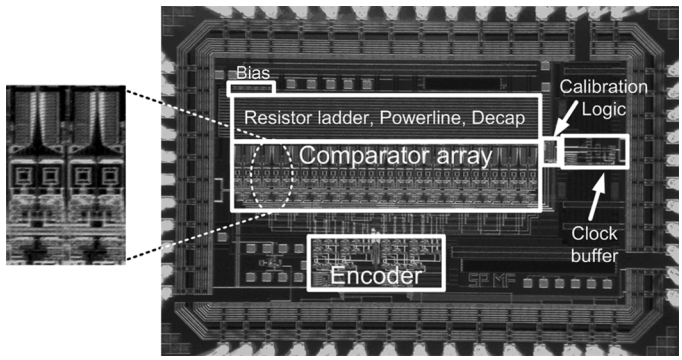

Fig. 15. ADC micrograph with a close-up view of four comparators.

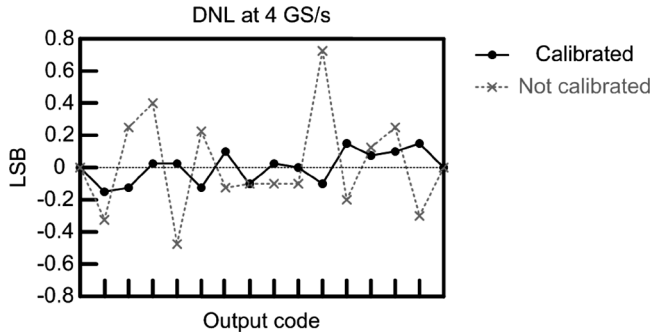

Fig. 16. DNL at 4 GS/s.

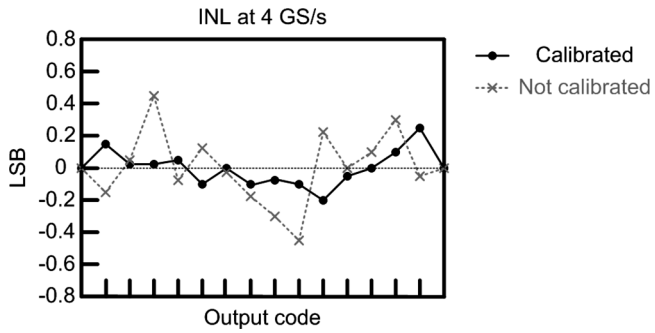

Fig. 17. INL at 4 GS/s.

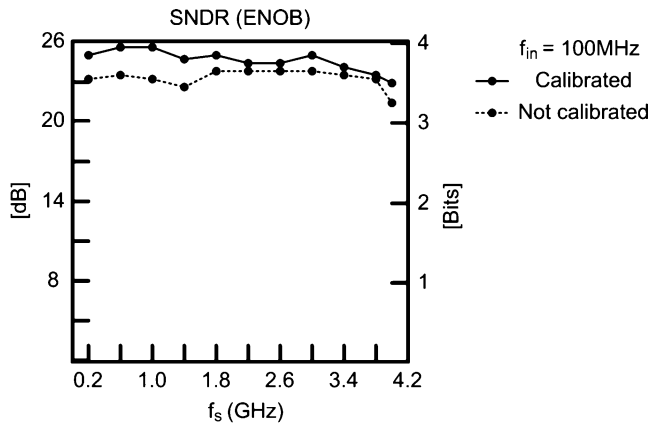

Fig. 18. SNDR versus sampling frequency (f_s) with 100 MHz input frequency (f_{in}).

circuit is not used. Each comparator set consists of two comparators (for redundancy), with each incorporating a differential inductor. Each comparator incorporates a trim DAC and a register that stores the offset calibration information. A Wallace tree counter [28] performs thermometer-to-binary conversion. Since the counter counts the number of digital 1s, its operation does not depend on the location of the 1/0 transition in the thermometer codes. Therefore, it is relatively resilient to bubbles, sparkles and metastability errors. To ensure operation of the counter at 4 GS/s in 0.18-μm CMOS, the encoder is implemented as two time-interleaved counters, running at half of the comparator clock frequency (i.e., 2 GHz at 4 GS/s). The counter is built with pipelined full adders for speed and both the full adders and D-FFs use differential digital inputs and outputs to achieve fast operation. The sampling clock V_{clk} is divided by 256 to generate the DAC clock, and by 2 to generate the counter clock. To facilitate testing of the prototype, the digital output of the encoder is decimated by 64.

VI. Measurements

The ADC was fabricated in 0.18-μm digital CMOS and packaged in a 52-pin LCC ceramic package. Fig. 15 shows a die photograph of the ADC. Including the 30 differential inductors, the total active area (excluding the resistor ladder) is 0.88 mm^2. The prototype runs off of 1.8 V analog and 2.1–2.5 V digital supplies (i.e., 2.1 V at 0.5 GS/s, 2.2 V at 2 GS/s, 2.3 V at 3 GS/s, 2.4 V at 3.4 GS/s, and 2.5 V at 4 GS/s). The higher digital supply compensates for a resistive voltage-drop due to a layout error in the digital power routing.

Fig. 16 and Fig. 17 show DNL and INL measured at 4 GS/s with a 10 MHz input. Measured DNL lies between -0.14 and 0.15 LSB, and INL is between -0.20 and 0.24 LSB, after calibration. Although DAC trimming and calibration, in principle, should set comparator offset to between 0 and -0.08 LSB, the accuracy of calibration is limited by device noise and reference noise.

Fig. 18 shows the measured SNDR versus sampling clock frequency (f_s) with a full power 100 MHz input (f_{in}). The measured ENOB is more than 3.48 effective bits at 4 GS/s after calibration. Fig. 19 shows the variation of SNDR versus input frequency (f_{in}) for three different sampling frequencies after

TABLE I
ADC PERFORMANCE SUMMARY

Technology	0.18 μm CMOS
Resolution	4 bits
Supply	Analog: 1.8 V Digital: 2.1–2.5 V
Input range	±460 mV_{pp}
Sampling rate	Up to 4 GS/s
Power – analog	78 mW
Power – digital, clock buffer	505 mW (3 GS/s, 100 MHz input) 633 mW (3 GS/s, 800 MHz input) 473 mW (3 GS/s, 1500 MHz input) 530 mW (4 GS/s, 100 MHz input)
DNL at 4 GS/s	–0.14 ~ 0.15 LSB (after calibration) –0.47 ~ 0.72 LSB (before calibration)
INL at 4 GS/s	–0.24 ~ 0.20 LSB (after calibration) –0.46 ~ 0.44 LSB (before calibration)
ENOB	3.89 bits (4 GS/s, 10 MHz input) 3.48 bits (4 GS/s, 100 MHz input) 3.47 bits (3.4 GS/s, 800 MHz input)
BER	$<10^{-11}$ (4 GS/s, 100 MHz input)
Active area	0.88 mm^2 (excluding resistor ladder)
Input capacitance	1.6 pF
Package	LCC52

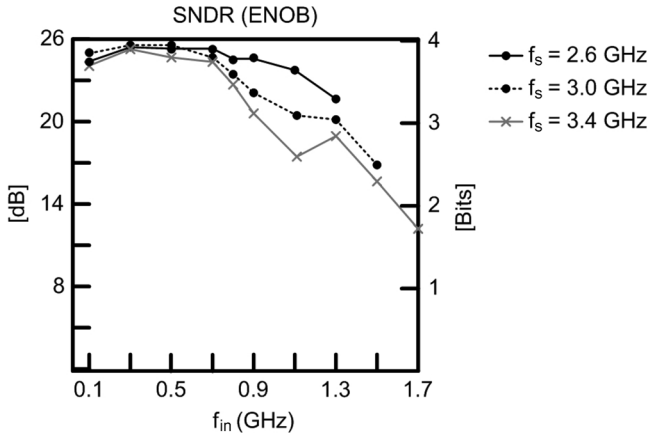

Fig. 19. SNDR versus input frequency ($f_{\rm in}$) with 2.6 GS/s, 3.0 GS/s, and 3.4 GS/s sampling frequencies (f_s).

calibration, with $f_{\rm in}$ up to the Nyquist rate for each sampling frequency. Jitter noise, clock skew, and package/pad loss dominate above $f_{\rm in} = 0.9$ GHz.[7] The ADC achieves an SFDR of 36.5 dB with $f_{\rm in} = 0.3$ GHz and $f_s = 2.6$ GHz, and 30.0 dB with $f_{\rm in} = 0.7$ GHz and $f_s = 3.4$ GHz. Using the method described in [29], no metastability error was detected in 10^{11} samples, indicating a BER less than 10^{-11}. The measured ENOB (with $f_{\rm in} = 0.3$ GHz, $f_s = 2.4$ GHz) from the 4 ADCs evaluated is between 3.75 and 3.91 bits. The analog circuitry (comparator core, regenerative stages, and resistor ladder) consumes 78 mW at 4 GS/s. Digital power consumption is proportional to f_s. Table I summarizes the ADC performance.

[7]Clock skew comes from mismatch in clock buffers, and clock distribution, and also threshold voltage mismatch of the comparator clock inputs. There is also degradation caused by bond wire mismatch, and the nonlinear capacitance of the input ESD diode.

VII. CONCLUSION

On-chip inductors improve the comparator reset and tracking mode time constants and the regeneration mode time constant, without any additional power consumption. Since the parasitic resistance of the inductors can be considered as part of the load resistors, the inductors consume little area. Two additional latches after the comparator core increase the overall voltage gain of the entire comparator, and reduce the probability of the metastability. To maximize the sampling rate, we use fast, minimum gate-length transistors in the high-speed signal path. The combination of comparator redundancy and DAC trimming corrects both static and dynamic offsets of the comparator core and of the subsequent latches. A prototype 4-bit flash ADC, built in 0.18-μm digital CMOS achieves a measured DNL and INL of less than one quarter LSB at 4 GS/s. The measured ENOB is 3.89 bits at 4 GS/s with a 10 MHz input, and 3.47 bits at 3.4 GS/s with an 800 MHz input.

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