A Fully Integrated Auto-Calibrated Super-Regenerative Receiver in 0.13-μm CMOS

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***Abstract*—Super-regeneration is re-examined for its simplicity and power efficiency for low-power, short-range communication. A fully integrated super-regenerative receiver in 0.13-μm CMOS is designed to operate in the 2.4 GHz ISM band. A frequency synthesizer scheme tunes the passband. Successive approximation register (SAR) logic driving a current digital-to-analog converter (DAC) calibrates the quench signal to enhance the selectivity of a Q-enhanced filter and the sensitivity of super-regeneration. A single-chip prototype receiver occupies less than 1 mm^2, has a turn-on time of 83.6 μs, a channel spacing of 10 MHz, and a sensitivity of -90 dBm. A data rate of 500 kb/s is achieved with a power consumption of 2.8 mW, corresponding to energy consumption of 5.6 nJ per received bit.**

***Index Terms*—Digital-to-analog converters, frequency synthesizer, low power consumption, super-regenerative receiver.**

I. Introduction

APPLICATIONS such as sensor networks, implantable neuroprosthetic devices, robotics, and home automation require power-efficient short-range wireless communication. For these applications a low data-rate is sufficient but long lifetime and small size are required. In the case of neuroprosthetic applications, the cost of frequently changing a battery is intolerable. In addition, the turn-on time of the receiver must be minimized to avoid wasting energy. To achieve these goals, the receiver architecture must be optimized to reduce power consumption and minimize turn-on time. In addition, the receiver should be self-sustaining and robust. Super-regeneration, a technique invented by Armstrong in 1922 [1], is a candidate architecture. In one of his super-regenerative radios, Armstrong used only two vacuum tubes to achieve a gain of more than 50,000 [1]. The extraordinary gain and simplicity of super-regeneration promise low-power consumption and small circuit area. However, super-regenerative receivers tend to be very sensitive to component accuracy, require high-Q passive components, and suffer from poor selectivity. In this paper, we describe a fully integrated, single-chip super-regenerative receiver which does not require off-chip passives. A novel calibration scheme greatly enhances the controllability and robustness of the receiver. Furthermore, calibration of frequency and bias current allows effective Q-enhanced filtering. The resulting receiver achieves an energy per received bit of 5.6 nJ/bit.

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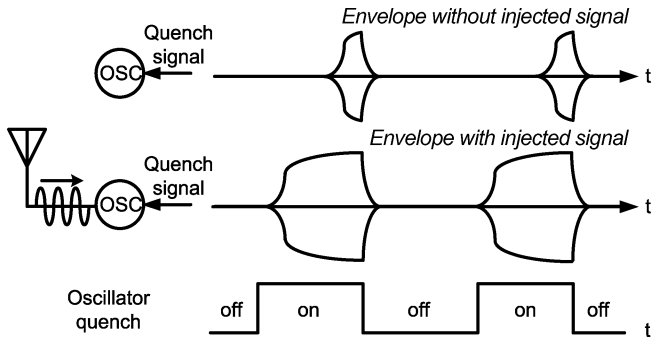

Fig. 1. Envelope of oscillation without (top) and with (middle) injected signal.

The basic idea behind super-regeneration is demonstrated in Fig. 1. In this example, two identical oscillators are powered up and down under the control of the same quench signal. Super-regeneration is based on the startup of an oscillator. The first example (top of Fig. 1) shows the start-up of a standalone oscillator. The oscillation envelope (i.e., the peak-to-peak amplitude) grows and decays with the quench signal. In the second case (middle of Fig. 1), an external signal (such as a signal received by an antenna) is injected into the oscillator causing the oscillation to start up much earlier. Since the difference in startup time depends on the strength of the injected signal, the oscillator can be used as a detector. However, once the oscillation saturates, we have to disable the oscillation to make use of the startup again.

In practice, super-regeneration suffers from poor selectivity since any injected signal might start an oscillation. To improve selectivity, the oscillator circuit is first configured as a Q-enhanced, bandpass filter, through control of the positive feedback in the oscillator. However, the resulting selectivity is very hard to achieve in a stable and repeatable manner, since the positive feedback changes with process, power supply voltage, and temperature. Previous integrated super-regenerative receivers require an off-chip signal to help tune this positive feedback, and also rely on a high quality off-chip resonant circuit, limiting both the size reduction and robustness of the receiver [2]–[5].

In the new scheme, instead of a simple periodic waveform such as a sawtooth or a sinusoid [2], a current-output digital-to-analog converter (DAC) applies an optimal quench waveform. This waveform is auto-calibrated to improve controllability and robustness. A novel calibration scheme tunes the

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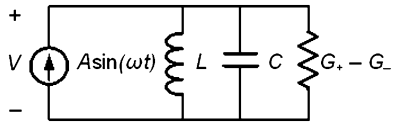

Fig. 2. Parallel resonant circuit representing an oscillator.

positive feedback to achieve Q-enhancement, with a measured resonator quality factor of more than 1000. A phase-locked loop (PLL) scheme tunes the frequency of a super-regenerative oscillator, setting the filter passband. Multi-channel operation is achieved by changing the PLL divider ratio. The combination of Q-enhancement, calibration and frequency tuning allows an on-chip LC tank to be used. A fully integrated 500 kb/s prototype device, fabricated in 0.13-μm CMOS, has a power consumption of 2.8 mW, corresponding to an energy per received bit of 5.6 nJ/bit.

II. Theory of Super-Regeneration

Super-regeneration is best understood by studying the parallel resonant tank which forms the core of a resonant oscillator, as shown in Fig. 2. The resonant tank consists of an inductor L, a capacitor C, and a shunt conductance $G_+ - G_-$. Here, G_+ represents the parasitic loss of the resonant circuit while $-G_-$ represents the negative conductance provided by active devices. The active devices compensate for loss in the tank, and the overall conductance $G = G_+ - G_-$ can be either positive or negative depending on the energy supplied by the active devices. An injected input signal is modeled by a sinusoidal current source $A\sin(\omega t)$.

Summing the currents in Fig. 2, we have

$$C\frac{dV}{dt} + GV + \frac{1}{L}\int V dt = A\sin(\omega t). \tag{1}$$

Solving for V, the complete solution of the voltage across the tank can be written as

$$V = e^{-\alpha t}(k_1 e^{j\omega_d t} + k_2 e^{-j\omega_d t}) + \frac{A\sin(\omega t + \phi)}{\sqrt{G^2 + (\omega C - 1/\omega L)^2}} \tag{2}$$

where the damping factor, $\alpha = G/2C$, is directly proportional to the conductance G and the damping frequency, $\omega_d = \sqrt{(1/LC) - (G/2C)^2} = \sqrt{(\omega_0^2 - \alpha^2)}$.

The first term in (2) is a transient oscillation at frequency ω_d with the damping factor α, representing the free response, and does not depend on the injected signal. If G is positive, the active devices do not provide enough energy to compensate for all the loss in the tank so that the free oscillation dies out and only the second term, which represents the forced response to the injected signal, remains. On the other hand, if G is negative, the active devices provide more energy than is dissipated in the resonant circuit, building up a free oscillation from an initial voltage. This special case is termed *super-regeneration*.

In order to detect the injected signal, we first make the conductance G positive, letting the free oscillation die out, and then change the conductance G from positive to negative. Thus, the initial voltage, at the moment that the total conductance turns

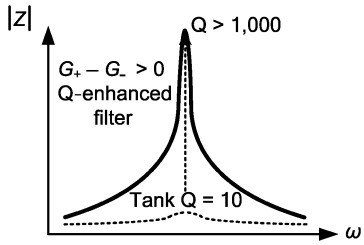

Fig. 3. Plot of impedance versus frequency with and without Q-enhancement.

negative, is solely determined by the forced response (i.e., the second term of (2)), which is proportional to the strength of the injected signal. Since the free oscillation begins from an initial voltage and its amplitude tends to grow towards infinity, this is a very effective way to achieve amplification. Once a free oscillation starts, the oscillation amplitude tends to grow regardless of the injected signal, and therefore to amplify and detect any subsequent input samples, it is necessary to reset any oscillation by periodically alternating the total conductance from negative to positive. Since an LC tank always has a certain positive conductance due to loss (i.e., G_+), we only have to control the negative conductance $-G_-$ to vary the sign and value of the overall conductance. The value of the negative conductance is controlled by the quench signal. The rate at which we alternate the total conductance is called the *quench frequency*.

From the above discussion, we can draw the following conclusions.

1) Amplification is achieved through the reinforcement of the free oscillation and this growth in oscillation amplitude requires time to build up. In order to achieve a larger gain, (represented by $e^{-\alpha t}$ in (2)), we either have to spend more time operating in super-regeneration or increase α by increasing the absolute value of the negative conductance.
2) The initial voltage of the free oscillation is proportional to the strength of the injected signal. Thus, it is straightforward to use super-regeneration to detect amplitude modulated (AM) signals.
3) The system does not continuously respond to the injected signal; it only responds as the conductance turns negative. Therefore, a super-regenerative receiver is a sampling system that samples the incoming RF signal with a sampling frequency equal to the quench frequency.

One major limitation of the super-regenerative technique is poor frequency selectivity, since an injected signal at any frequency might cause a free oscillation. However, since the free oscillation in super-regeneration starts with an amplitude determined by the forced response, which has a bandpass characteristic (second term in (2)), the system can inherently provide a bandpass frequency response. Without active devices, the quality factor Q of the resonant tank is

$$Q = \frac{1}{G_+}\frac{1}{\sqrt{L/C}}. \tag{3}$$

An on-chip LC tank normally has a quality factor of 10 or less and, therefore, offers poor frequency selectivity. However, we can significantly improve frequency selectivity through Q-enhancement. As shown in Fig. 3, Q-enhancement is achieved by

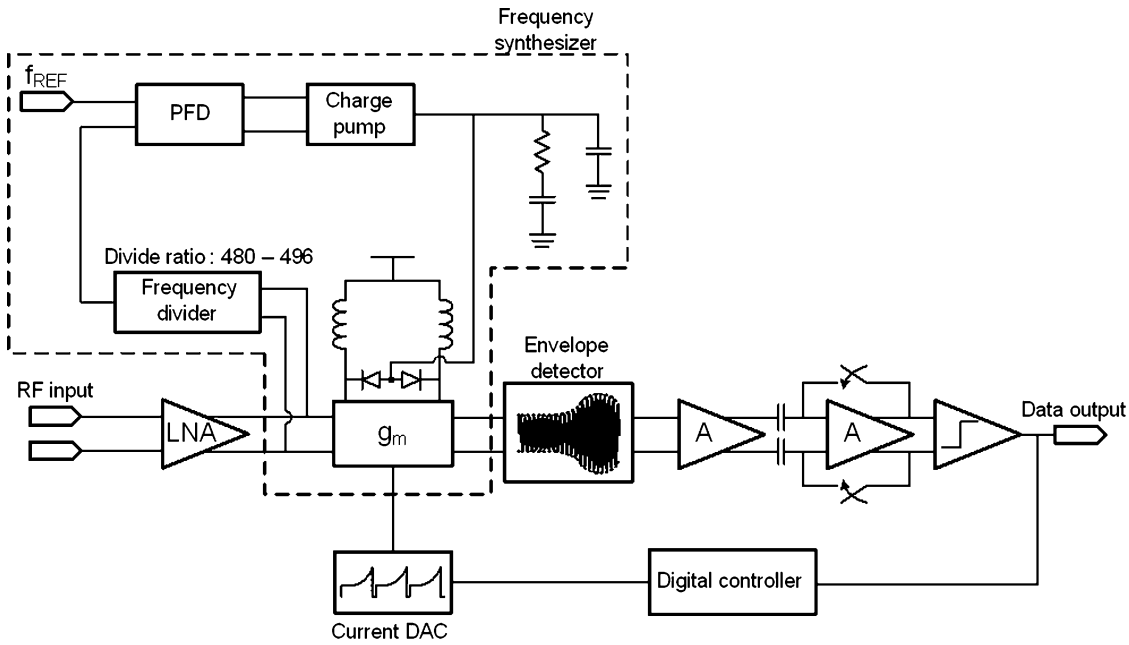

Fig. 4. Architecture of the prototype receiver.

using the negative conductance G_- to cancel some of the positive conductance G_+, while keeping the overall conductance G positive. The resulting enhanced Q can be expressed as [6]

$$Q_{en} = \frac{1}{G_+ - G_-}\frac{1}{\sqrt{L/C}}. \tag{4}$$

In summary, we first operate the circuit as a Q-enhanced bandpass filter to select the band of interest. Next, we increase the negative conductance to achieve super-regeneration and amplify the selected signal. The initial condition for super-regeneration is set at the moment when the overall conductance turns negative. Therefore, by periodically controlling the negative conductance, operating the circuit first in the Q-enhanced mode and then in the super-regenerative mode, we detect the signal sampled at the quench frequency.

III. Receiver Architecture

A. System Architecture

Fig. 4 shows the architecture of the prototype receiver. The prototype receiver incorporates a low-noise amplifier (LNA), a voltage-controlled oscillator (VCO), a DAC current source that provides the bias current for the VCO, an envelope detector, a pre-amplifier, a comparator, a frequency synthesizer (which shares the same VCO), and a digital controller. The super-regenerative oscillator, described in the previous section, is realized as a VCO. In normal operation, the incoming RF signal is amplified by the LNA, the input of which is matched to 50 Ω at 2.4 GHz, and then directly injected onto the oscillatory nodes of the VCO. The current output DAC supplies the bias current of the VCO, controlling the negative conductance generated by the active devices. The bias current is periodically varied so that the circuit selects and amplifies the sampled RF signals. The envelope detector senses the oscillation envelope and its outputs are fed to a preamplifier and a comparator. The comparator determines if and when the oscillation occurs and generates the corresponding digital data to reflect the strength of the detected signal. Before normal operation begins, the system calibrates the oscillator bias current and frequency. Frequency calibration is achieved by temporarily configuring the VCO as part of a frequency synthesizer loop. A digitally controlled successive approximation search calibrates the bias current.

B. Frequency Tuning and SAR Auto-Calibration

The receiver first operates in a frequency-tuning mode to set the center frequency of the passband. Frequency tuning is required since the narrow, Q-enhanced passband is sensitive to process, temperature and supply voltage changes. Frequency tuning also facilitates multi-channel operation. A programmable integer-N PLL adjusts the varactor voltage, tuning the frequency of the VCO and resonant frequency of the tank. The frequency divider is programmable, allowing any one of nine channels to be selected. Once frequency tuning is complete, the frequency synthesizer is powered down and the varactor tuning voltage is held on the large grounded capacitor of the PLL loop filter. Since this tuning voltage is subject to leakage (e.g., through the open charge-pump switches) frequency tuning needs to be performed periodically. The target applications typically have a short duty cycle of operation, and frequency tuning need only be performed before receiving a burst of data.

After the passband is tuned, the VCO can serve as a filter or as a super-regenerative oscillator, depending on the balance between the energy provided by the active devices and the loss of the tank. For a cross-coupled LC oscillator, the negative conductance provided by the active devices is $-g_m/2$, where g_m is the transconductance of each of the cross-coupled devices and it is related to the MOS drain current [7]. The bias current at which the negative conductance exactly compensates the loss in

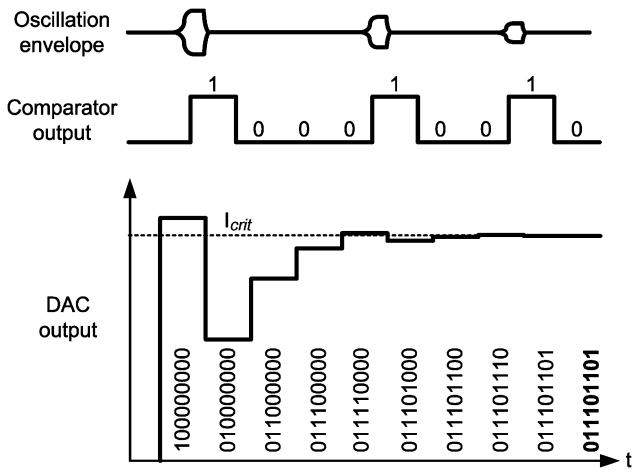

Fig. 5. $I_{\rm crit}$ search with SAR algorithm.

the resonant tank is called the critical current $I_{\rm crit}$. The VCO operates as a filter for bias current below $I_{\rm crit}$ and as a super-regenerative oscillator for bias current values above $I_{\rm crit}$. For an on-chip resonant tank, the exact value of loss is difficult to determine; furthermore, $I_{\rm crit}$ varies with temperature, resulting in inconsistent receiver selectivity and sensitivity.

We employ the successive approximation register (SAR) algorithm [8] to determine the value of $I_{\rm crit}$. As shown in Fig. 5, the 9-bit DAC quench waveform generator first sets the bias current to midscale (i.e., MSB $=1$) and the SAR logic reads the comparator output, checking for oscillation, to determine if this current value is larger than $I_{\rm crit}$. The binary search continues to determine the full 9-bit bias current that is closest to, but below, $I_{\rm crit}$. This value of bias results in the maximum enhanced Q. Once $I_{\rm crit}$ is known, the digital controller can generate the corresponding quench waveform to maximize both selectivity and sensitivity.

C. Quench Mechanism

In a super-regenerative receiver, an oscillator is turned on and off at the quench rate, sampling an RF signal. As described in Section II, the negative conductance from the active devices is controlled periodically to filter and then amplify the RF signal. Since the negative conductance is proportional to the bias current of an oscillator, the periodic quench signal that controls the bias current of the oscillator needs to be carefully designed to optimize the receiver performance. This quench waveform is traditionally limited to sinusoidal, sawtooth, triangular and rectangular waveforms [2] since these waveforms are relatively easy to generate. However, given the ability to generate arbitrary waveforms, certain shapes exist which lead to better gain and selectivity. Instead of using a simple quench signal [2]–[5], we use an on-chip current DAC to generate the arbitrarily shaped quench bias current waveforms for the oscillator. As described above, $I_{\rm crit}$ is chosen as the minimum DAC current value that results in oscillation. Once $I_{\rm crit}$ is known, the quality factor of the tank is maximized, enhancing the selectivity of the bandpass filter, by setting the current DAC just one LSB below $I_{\rm crit}$.

Fig. 6 shows the quench waveform generated by the current DAC. During each detection period, the bias current is first set to just below $I_{\rm crit}$ so that the circuit operates in the Q-enhanced

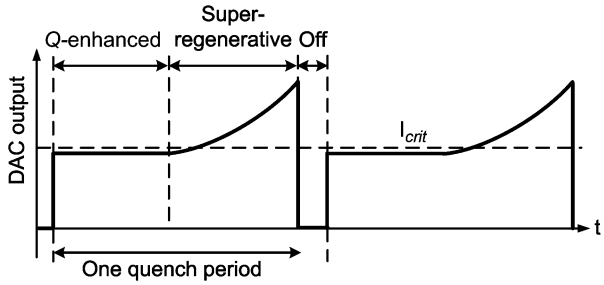

Fig. 6. The quench current waveform generated by the DAC.

mode, suppressing out-of-band signals. Next, the bias current is first increased slowly past $I_{\rm crit}$ and then more rapidly with time, to achieve both a smooth transition from Q-enhancement to super-regeneration and sufficient gain to amplify the input signal. At the end of each cycle, the bias current is turned off, disabling any oscillation. This complex quench waveform can be easily generated and calibrated by the current DAC under control of the digital controller.

D. Timing Diagram

Fig. 7 shows the timing diagram of the receiver and the quench waveform. Although frequency tuning is performed before the critical current search, a coarse critical current search is performed initially to determine a proper bias for the VCO during frequency tuning. (During frequency tuning the VCO bias is set somewhat higher than the critical current to ensure oscillation.) The receiver then tunes the tank frequency by configuring the oscillator as part of a frequency synthesizer. Since the initial critical current search is performed before setting the proper tuned varactor voltage, the system runs the SAR algorithm critical current search again to accurately determine the value of $I_{\rm crit}$. In detection mode, each detection period spans 10 clock cycles of the 5 MHz system clock. During the first four cycles, the receiver operates as a Q-enhanced filter. During the next five cycles, with an exponentially growing bias current, it operates in the super-regenerative mode for signal detection, Finally, during the last cycle, the oscillator's bias current is turned off, quenching any oscillation. The comparator is enabled during the last six cycles and its output becomes logic 1, if and when, the VCO oscillates. The number of 1's in the data output per detection period is a measure of the startup time, and reflects the detected strength of the incoming RF signals. With a 5 MHz clock, the quench frequency is 500 kHz, and the resulting data rate is 500 kb/s.

IV. Circuit Building Blocks

In this section, we discuss the key building blocks used in the prototype receiver.

A. Low-Noise Amplifier and Voltage-Controlled Oscillator

A low-noise amplifier provides input matching and improved isolation for the oscillator. One might wonder if the LNA could be completely eliminated from the system. Recalling the system architecture, the LNA also serves as a buffer between the antenna and the oscillator. Ideally, we want the injection signal source to have infinite output impedance, as is the case with an ideal current source. Without an LNA, the 50-Ω antenna

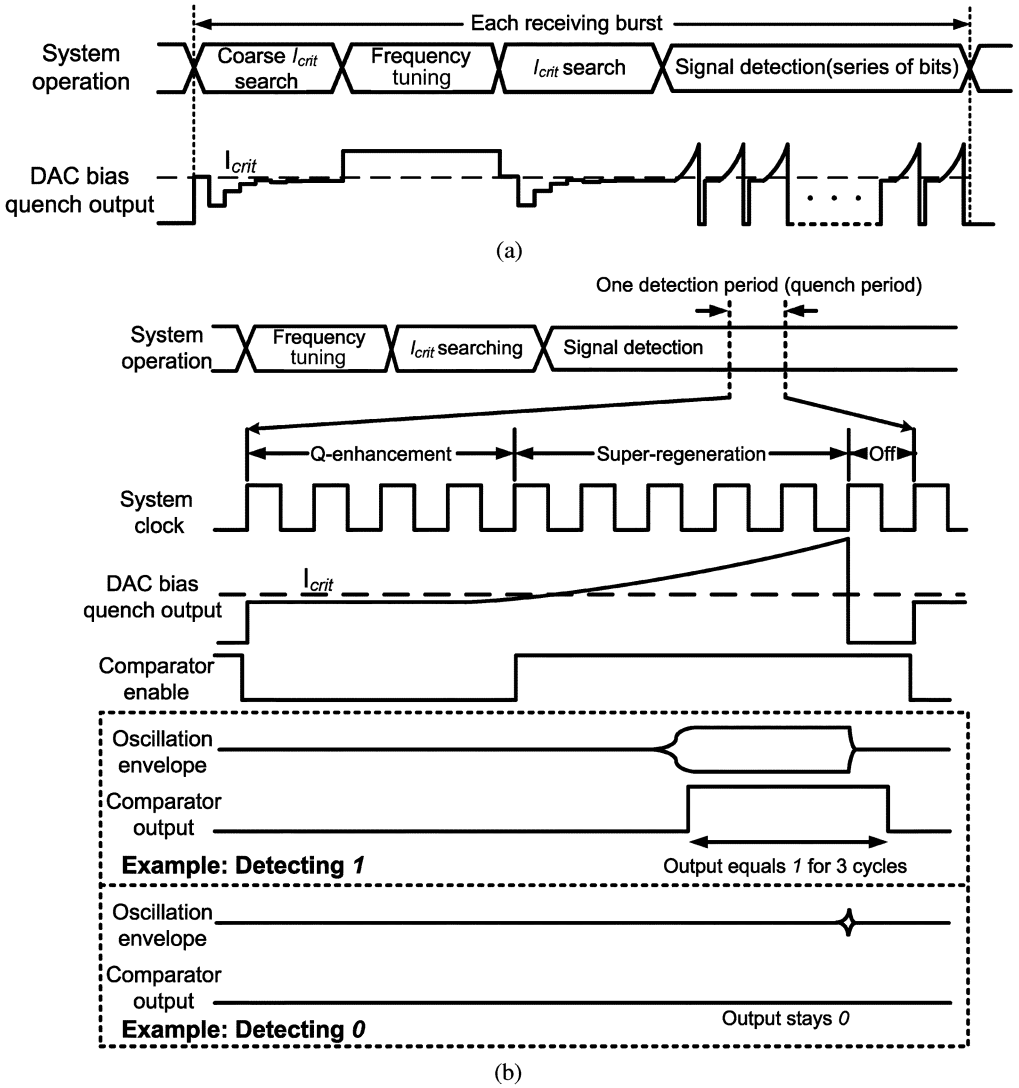

Fig. 7. Receiver timing diagram. (a) During each receiving burst. (b) Magnified diagram for one detection period.

impedance would directly load the resonant tank, dramatically lowering the tank Q.

The schematic of the LNA and VCO is shown in Fig. 8 [9]. An external balun transforms the singled-ended signal from the antenna to differential-ended. The RF inputs are AC-coupled to the LNA. As can be seen in Fig. 8, the LNA output current is directly injected into the oscillator, so that the resonant tank forms the load of the LNA. The cascode transistors M3 and M4 help present a high impedance to the resonant tank, preventing the quality factor from being degraded. The cascode transistors also improve isolation. Since the LNA is directly connected to the oscillator, oscillator leakage might otherwise be radiated through the antenna. All the inductors in this LNA are on-chip spiral inductors, except for the two inductors L_g which are realized with a combination of on-chip spiral inductors and bond wire inductance.

As mentioned earlier, we implement the super-regenerative oscillator as a VCO to enable frequency tuning. As also shown in Fig. 8, the inductors are implemented on-chip, and a pair of junction varactors tune the frequency. The outputs (nodes X and Y) are connected to an envelope detector to sense oscillation. The cross-coupled transistors, M7 and M8, provide a negative conductance $-g_m/2$ which is adjusted by changing the bias current, modifying the overall conductance of the resonant tank as discussed above. To reduce power consumption, a large W/L ratio is desirable since this results in a larger g_m for a given bias current, but on the other hand transistor size is limited by noise and loading. Since the super-regenerative VCO serves as an amplification device, rather than a signal source, phase noise is not critical but the amplitude noise during the startup period can affect the startup time of the oscillation. On the other hand, during Q-enhancement mode, the super-regenerative oscillator acts like an active filter, and the contribution of the noise during this period can be overcome by the gain of the LNA. The noise referred to the input of the LNA can be expressed as (we only consider the thermal noise of M1, M2, M7, and M8 in Fig. 8)

$$\overline{v_n^2} = 4kT\gamma \frac{1}{g_{mM1,2}} \left(1 + \frac{g_{mM7,8}}{g_{mM1,2}}\right). \tag{5}$$

Therefore, the g_m provided by M7, M8 should be lower than that provided by M1, M2 to prevent the noise of the oscillator from dominating the overall noise of the receive path in the super-regenerative receiver.

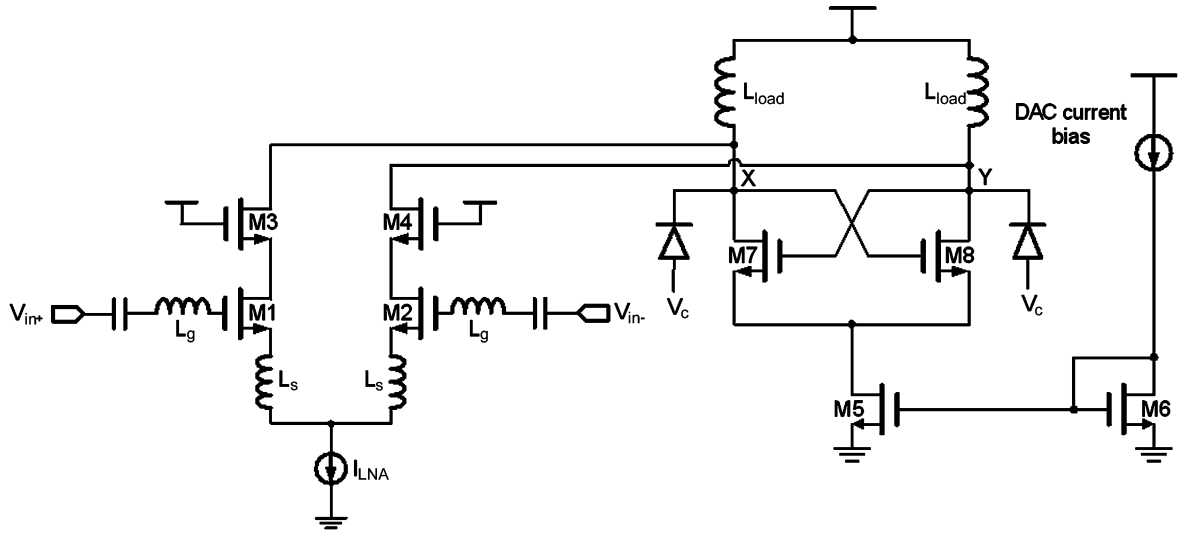

Fig. 8. Schematic of the fully differential inductive-degeneration LNA and the super-regenerative VCO.

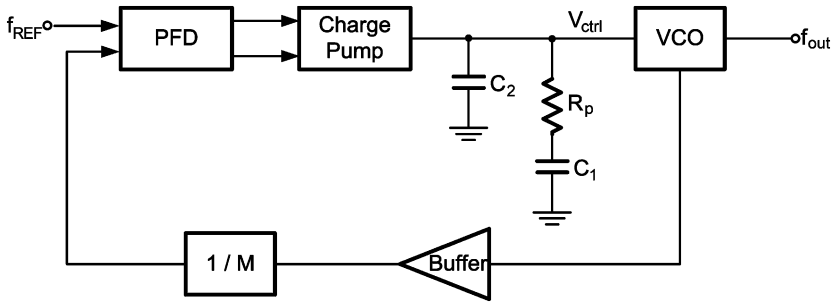

Fig. 9. The integer-N frequency synthesizer implemented in the prototype.

B. Frequency Synthesizer

In this design, we use a frequency synthesizer to set the passband to the desired channel by tuning the center frequency of the resonant tank. Fig. 9 shows the architecture of the integer-N frequency synthesizer implemented in this prototype. It consists of a phase frequency detector (PFD), a charge pump, a loop filter, a VCO, a buffer and a divider.

A buffer between the VCO output and the frequency divider converts the oscillator output to a rail-to-rail amplitude, so that the digital divider can properly process the signal. A block diagram of the programmable frequency divider is shown in Fig. 10 [10]. As shown in the figure, the divider consists of a divide-by-two circuit (implemented with a true-single phase clocked flip-flop [11]), a prescaler, a programmable counter, and a swallow counter. The divide ratio is expressed as

$$ratio = 2\times((60-S)\times 4+5\times S) = 2\times(60\times 4+S) \quad (6)$$

where S = 0–8, providing a divider ratio ranging from 480 to 496 with a spacing of 2. With a 5 MHz reference clock, the frequency synthesizer locks the tank center frequency from 2.4 GHz to 2.48 GHz, in increments of 10 MHz.

C. Current Output Digital-to-Analog Converter (DAC)

Since the precision of the bias control directly affects the system performance, a 9-bit current steering DAC with an LSB size of 2 μA, and a full-scale output current of 1024 μA, sets the bias current of the VCO. Monotonicity is important to ensure a correct search for the critical current and also to ensure smooth growth of bias current during signal detection. A segmented architecture [11] is adopted to guarantee monotonicity, yet minimize complexity. As shown in Fig. 11, the 3 MSBs are thermometer-coded and the 6 LSBs are binary-coded.

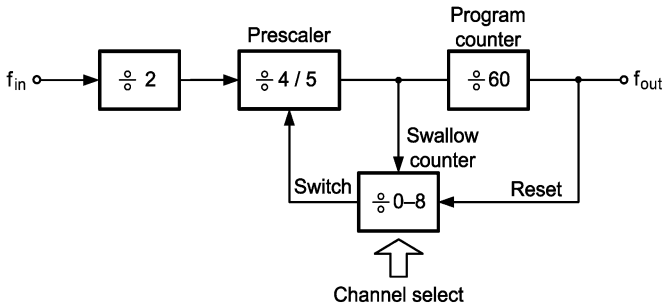

Fig. 10. Block diagram of the programmable frequency divider [12].

D. Envelope Detector

A simple envelope detector, shown in Fig. 12, monitors the oscillation startup. The circuit on the left-hand side of Fig. 12 is a peak detector and its differential inputs, $V_{\rm inp}$ and $V_{\rm inn}$, are connected to the outputs of the VCO (nodes X and Y in Fig. 8). The circuit on the right of Fig. 12 is a replica circuit without source load capacitor and with its inputs (the gates of M11 and M12)

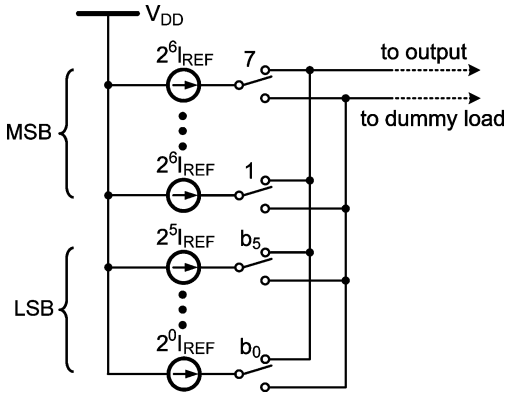

Fig. 11. Segmented architecture of the 9-bit current steering DAC.

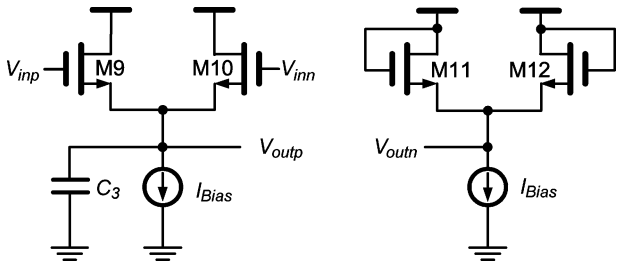

Fig. 12. Schematic of the envelope detector, showing the peak detector and replica circuit.

connected to VDD. If the VCO does not oscillate, the oscillatory nodes remain at the supply voltage, and the output voltage of the peak detector $V_{\rm outp}$ remains the same as the output $V_{\rm outn}$ of the replica circuit. Once the VCO begins to oscillate, the source voltages of M9 and of M10 follows the peak oscillator differential voltage, pulling the voltage on the capacitor C3 high. M9 and M10 are biased in the subthreshold region to achieve larger detection gain while consuming very little power [13].

Note that, in order to track the envelope of the $\sim$2.4 GHz oscillation while operating in the subthreshold region, the capacitance at $V_{\rm outp}$ cannot be too large, and in practice, M9–M12 should be small to reduce loading at $V_{\rm outp}$. However, mismatch in threshold voltages of small transistors M9–M12 can introduce a large offset voltage so that, even in the absence of oscillations, the voltages at $V_{\rm outp}$ and $V_{\rm outn}$ differ because of differences in the gate-source voltages of M9–M12. To accurately measure the oscillation envelope, we use an offset-cancelled preamplifier to store the offset voltage while the oscillator is disabled and cancel this offset voltage during normal operation (described in the next subsection).

E. Offset-Cancelled Preamplifier and Comparator

As shown in Fig. 13, a two-stage, offset-cancelled pre-amplifier and a comparator are used to determine if and when oscillation occurs. This circuit detects the change of the oscillation envelope when oscillation starts. The comparator [14] compares the oscillation amplitude with a reference voltage $V_{\rm Ref}$ that defines a minimum threshold for the oscillation envelope (generating an output of logic 1 if oscillation is detected). In order to cancel offsets introduced at the envelope detector, the switches

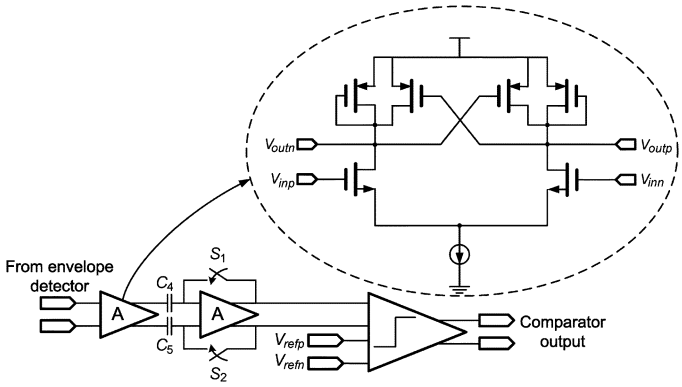

Fig. 13. Block diagram of the two-stage offset-cancelled pre-amplifier and a comparator.

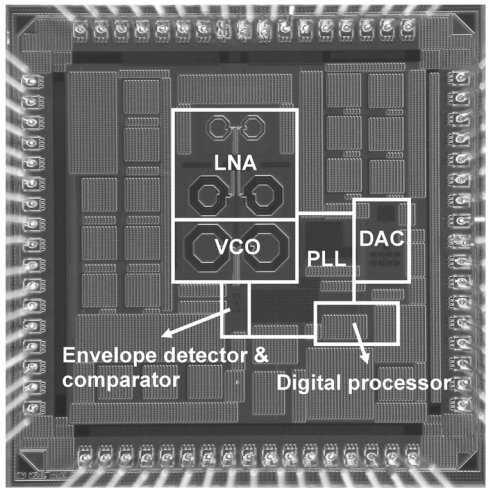

Fig. 14. Photomicrograph of the receiver prototype.

S_1 and S_2 are closed when the oscillator's bias is turned off, disabling any oscillation and storing the offset voltage on C_4 and C_5. Next, the switches are opened to detect the true oscillation envelope. To prevent gain saturation of the first amplifier stage of the pre-amplifier, the first stage must have a low gain [15]. This configuration also reduces the input offset voltage of the following comparator since the input referred offset voltage of the comparator is scaled down by the total gain of the two-stage pre-amplifier.

V. Measurement Results

The receiver prototype is fabricated in 0.13-μm CMOS technology. A photomicrograph of the receiver die is shown in Fig. 14 and the active circuit area is 1 mm^2. The device is packaged in a 68-pin LCC package and surface-mounted on a test PCB. We use a board-mounted off-chip balun to convert the single-ended RF input signal to a differential signal. The measured tuning range of the VCO is from 2.35 to 2.53 GHz, which covers the ISM band. The measured input reflection S_{11} is less than -12 dB over the entire ISM band (Fig. 15). We first measured the detected strength versus input power, for both the desired and the adjacent channels (10 MHz offset) input RF signals as shown in Fig. 16. As mentioned above, the number of 1's per detection period reflects the startup time and is an

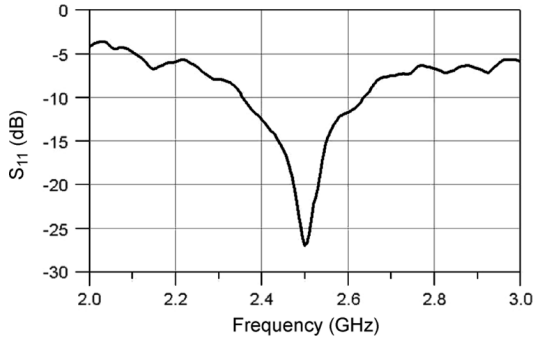

Fig. 15. Measured S_{11} versus input frequency.

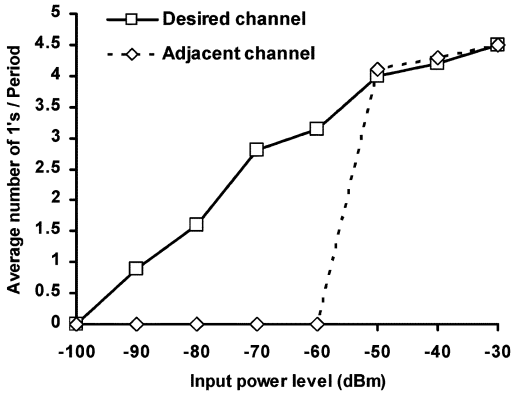

Fig. 16. Detected strength versus input power for the desired and adjacent channel signals.

indication of detected signal strength. We first observe from the figure that the detected strength increases with the input power level and the prototype is able to detect the desired channel signal when the input power is above -90 dBm. To appreciate the selectivity provided by this receiver, we look at the detected strength with an adjacent channel signal input. As shown in the figure, the detected strength is zero until the input power level is above -60 dBm, showing more than 30 dB of adjacent channel signal rejection.

As shown in Fig. 17, with a 1.2 V supply, signal rejection is -10 dB at a 3 MHz frequency offset. From this we calculate the enhanced Q of the on-chip resonant circuit to be approximately 1400. We also measured the selectivity under different supply voltages and the result is also shown in Fig. 17.

To evaluate the prototype at higher data rates, we increased the system clock frequency from 5 MHz to 10 MHz, corresponding to an increase in the quench frequency from 500 kHz to 1 MHz. As shown in Fig. 18, the minimum sensitivity increases from -90 dBm to -60 dBm, because of the reduced time allowed for oscillation to build up. In addition, signal rejection is roughly halved since the time for Q-enhancement is also reduced. Because the Q-enhanced filter does not have enough time to reach the steady state, the filtering response is degraded.

Fig. 19 shows BER measurements for 500 kb/s pseudo-random non-return-to-zero (NRZ) data modulated on a 2.45 GHz RF carrier. The measured BER is 0.1% for a -80 dBm input and becomes 6.5% for a -90 dBm input. The entire receiver, with the PLL reactivating every 100 ms, draws 2.4 mA which corresponds to 5.6 nJ per received bit at a data

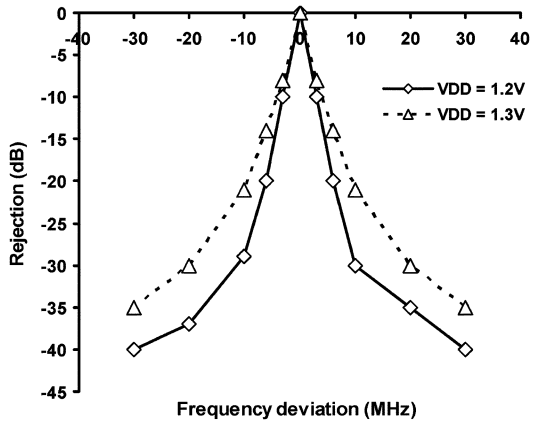

Fig. 17. Signal rejection at 2.45 GHz center frequency under different supply voltages.

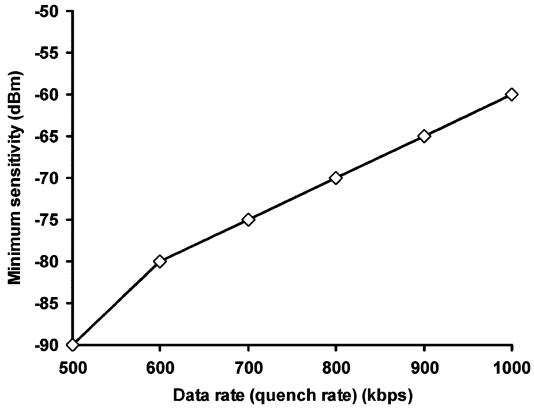

Fig. 18. Minimum sensitivity versus data rate for 2.45 GHz center frequency.

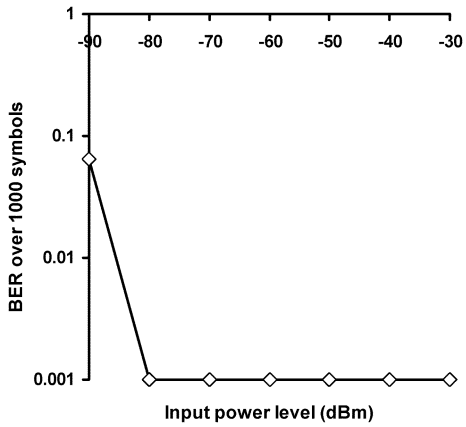

Fig. 19. BER versus input power at 2.45 GHz center frequency.

rate of 500 kb/s. The peak current consumption of 3 mA occurs when the PLL is operating—the extra current is mainly due to the consumption of the frequency divider and charge pump. The measured receiver performance is summarized in Table I.

VI. Conclusion

Super-regenerative receivers are suitable for low-power, short-range wireless communication, where a high data rate is not required. We have described one of the first super-regenerative receivers that implements all the RF, analog and

TABLE I
SUMMARY OF THE MEASURED PERFORMANCE FOR THE PROTOTYPE RECEIVER

Supply voltage	1.1 to 1.3 V
Power consumption	2.8 mW @ 1.2 V
VCO tuning range	2.35 to 2.53 GHz
Channel spacing	10 MHz
Circuit area	1 mm^2
Selectivity	900 kHz @ –3 dB (Q = 1400)
Sensitivity	–80 dBm
Data rate	500 kbps @ 500 kHz quench
BER (≥ –80 dBm input)	≤ 0.1 %
Turn-on time	83.6 μs
Energy per received bit	5.6 nJ @ 500 kHz quench

TABLE II
PERFORMANCE COMPARISON OF SEVERAL SUPER-REGENERATIVE RECEIVERS

	Vouilloz [4]	Otis [5]	Moncunill-Geniz [16]	This work
RF frequency	1 GHz	1.9 GHz	2.4 GHz	2.4 GHz
Sensitivity	–107.5 dBm	–100.5 dBm	–90 dBm	–90 dBm
Data rate	100 kbps	5 kbps	115.2 kbps	500 kbps
Bit error rate	0.1 %	0.1 %	0.1 %	0.1 %
Power consumption	1.2 mW	400 μW	2.7 mW	2.8 mW
Energy per bit	12 nJ/bit	80 nJ/bit	23 nJ/bit	5.6 nJ/bit
Quench signal	External analog sawtooth	External digital square	External analog sinusoidal	Internal digital
Tank	Discrete inductors	BAW resonator	Microstrip line	On-chip
Technology	0.35 μm CMOS	CMOS	Descrete BJTs	0.13 μm CMOS

digital functionality on a single chip. The issues which arise from integrating on-chip inductors are resolved by a novel auto-calibration scheme that combines a digital controller and a current DAC to dynamically adjust the operating point of the super-regenerative receiver and optimize performance, without any external control. Table II compares the performance of several recently published super-regenerative receivers, including this work. This single-chip design achieves an energy per received bit of 5.6 nJ/bit. The turn-on time of the prototype receiver is only 86 μs, smaller than that of most commercial receivers (usually > 250 μs) [17], [18].

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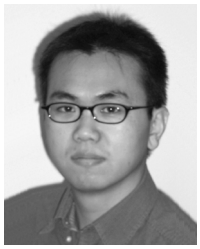

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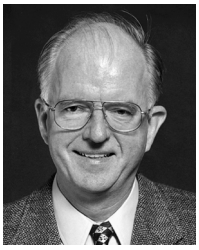

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