A 0.3mm^2 Miniaturized X-Band On-Chip Slot Antenna in 0.13µm CMOS

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***Abstract* — An on-chip miniaturized slot antenna integrated with a CMOS LNA, on the same chip, is presented in this paper. The antenna operates in the 9-10GHz frequency band, occupies a die area of only 0.3mm^2, and is fabricated in a standard 0.13µm RF CMOS process. A LNA implemted on the same substrate is directly matched to the antenna. An efficient shielding technique is used to shield the antenna from the low-resistivity substrate underneath it. Measurement results of the fabricated prototype indicate that the antenna shows an active gain of -4.4 dBi and an efficiency of 9% in spite of its close proximity to the lossy silicon substrate.**

***Index Terms* — Mobile antenna, integrated antenna, CMOS active antenna, receiving antennas, slot antennas.**

I. Introduction

Integration of an antenna with the rest of a transceiver on a single IC is perhaps the last barrier to achieving a totally integrated single-chip wireless system. Over the past few years, a number of researchers have attempted to address this increasingly important problem [1]-[4]. These studies report on using basic dipole-type on-chip antennas operating in frequency bands ranging from 7.4GHz to 77GHz. In all of these studies, the on-chip antennas are fabricated in standard CMOS processes and they demonstrate very low radiation efficiencies. This is mainly a consequence of the close proximity of the antenna to the lossy silicon substrate underneath it. This excessive loss significantly deteriorates the gain and radiation efficiency of these antennas. In this paper, we present a miniaturized, on-chip slot antenna operating in the 9-10GHz frequency band. This antenna has a much higher gain and efficiency compared to state-of-the-art on-chip antennas operating in a similar frequency range. Two main factors contribute to this enhanced performance: the choice of a slot-type antenna (as opposed to a dipole-type antenna) and the effective shielding of the antenna from the low resistivity silicon substrate. A prototype antenna was designed and implemented in a standard 0.13µm RF CMOS process. The antenna occupies a die area of only 0.3mm^2, has a measured active gain of -4.4dBi at 9.3GHz, and measured efficiency of 9%. The antenna alone, without the integrated LNA, achieves a measured gain of -10.0dBi.

II. On-Chip Integrated Antenna Design

Slot antennas can be considered to be dual of dipole- or wire-type antennas. For the same occupied area, slot antennas have a much larger metal area compared to wire-type antennas, since everywhere, except the antenna aperture, is covered with metal. In this way, the radiating currents are distributed over a larger metallic area and hence, the Ohmic losses in a slot antenna are significantly smaller than those in dipole or other wire-type antenna. In miniaturized antennas, where the radiation resistances are usually very small, even small changes in Ohmic losses have major implications on the radiation efficiency of the antenna. Therefore, by using a miniaturized slot topology, the radiation efficiency of small on-chip antennas can be significantly enhanced.

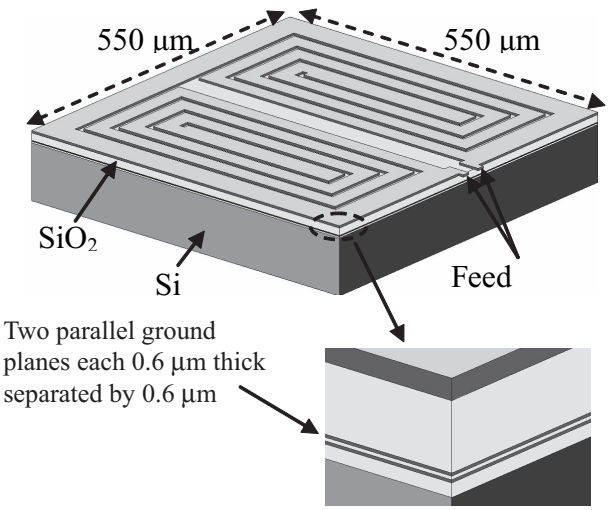

Fig. 1. Topology of the proposed miniaturized on-chip slot antenna. The antenna and shielding are implemented with standard RF interconnect layers.

The topology of the proposed on-chip slot antenna is shown in Fig. 1. Fig. 2 shows the top view of the slot antenna. The antenna is composed of a straight slot section connected to two balanced spirals at its end. The antenna is designed such that its overall electrical length, from the feed point to the end of each balanced spiral, is about a quarter of a wavelength ($\lambda/4$) at the center frequency of operation. This way, this structure acts as a resonant monopole slot antenna and occupies a significantly smaller area compared to traditional dipole or slot antennas. The two feed terminals of the antenna are located at its center, as shown in Fig. 2. In the current design, these two terminals are connected to the input of the LNA using vias. The antenna occupies a die area of only $0.3mm^2$ and operates in the frequency range of 9-10 GHz. The electrical dimensions of the antenna are $0.017\lambda_0 \times 0.017\lambda_0$, making it 30 times smaller than traditional dipole or slot antennas operating at the same frequency band.

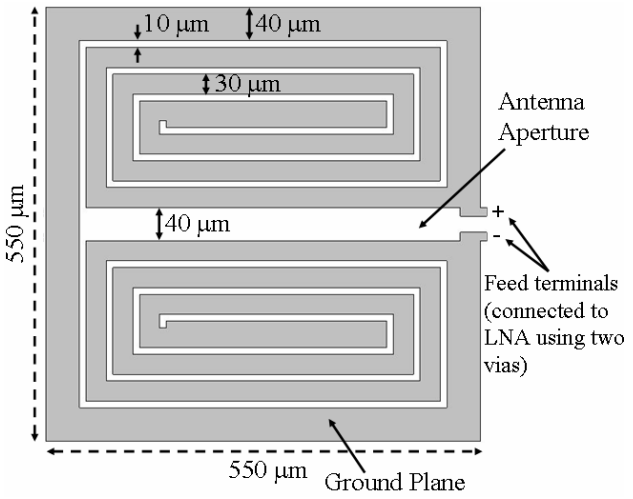

Fig. 2. Top view of the miniaturized on-chip slot antenna fabricated on the top metal layer of the 0.13μm process. The feed terminals are located at the center of the antenna and are connected to the LNA using two vias.

To shield the antenna from the low-resistivity silicon substrate below it, a composite ground plane is used underneath the antenna. This low-resistivity ground plane significantly reduces the adverse affects of the lossy substrate on the performance of the antenna. Presence of the ground plane prevents the fields from penetrating deep into the lossy silicon substrate and reduces the field density in the lossy regions nearby the antenna. This prevents the substrate from dissipating the power that would otherwise have been radiated, hence increasing the radiation efficiency of the antenna.

The slot antenna is fabricated on the highest of the metal layers available in the CMOS process. The 4μm thick aluminum top layer has the lowest surface resistivity. The lower metal layers that are used to implement the shielding ground plane are much thinner (0.6μm) and have a much higher surface resistivity. In order to circumvent the adverse affects of the high resistivity of these metal layers on the efficiency of the on-chip antenna, the shielding ground plane is composed of two floating individual ground planes placed on two lower metal layers. These layers, each 0.6μm thick, are separated by a 0.6μm oxide layer. This way, the capacitance between the two metal layers is large enough such that they act as a single ground plane with a much lower surface resistivity and there is no need to physically connect the two floating metallic layers with multiple vias. The antenna layout fully meets the stringent metal fill and density requirements of the 0.13μm process.

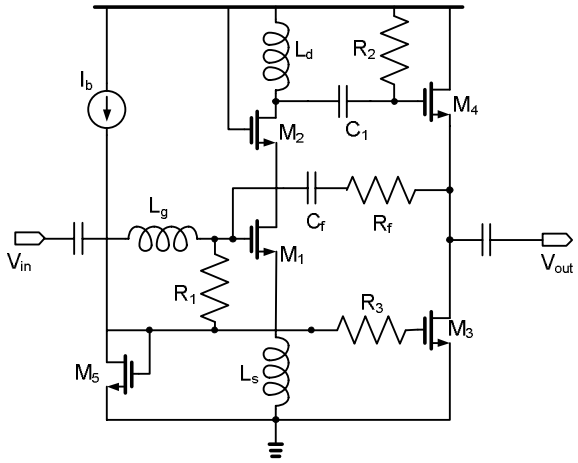

Fig. 3. Low noise amplifier (LNA) integrated with the miniaturized on-chip antenna.

The prototype IC incorporates a low noise amplifier (LNA) connected to the antenna, demonstrating that the antenna can function alongside CMOS RF circuitry. A schematic of the LNA is shown in Fig. 3. A common-source-LNA with inductive degeneration, which achieves noise matching and power matching using passive components, is employed. The LNA input is matched to the 50Ω input impedance of the antenna. Transistor M5 with resistors R1 and R3 provides a DC bias for the LNA input and the output buffers. To allow for simulation inaccuracy and process variation, feedback (consisting of Cf and Rf) is used to widen the bandwidth of the LNA. DC blocks are used at the input, the output and between the LNA core and the buffer to achieve proper bias

conditions. The LNA dissipates 15mW from a 1.2V supply.

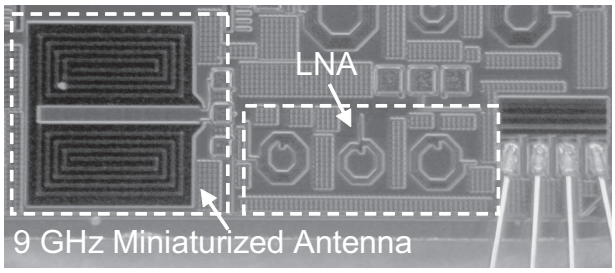

Fig. 4. Microhotograph of the on-chip antenna and the integrated LNA.

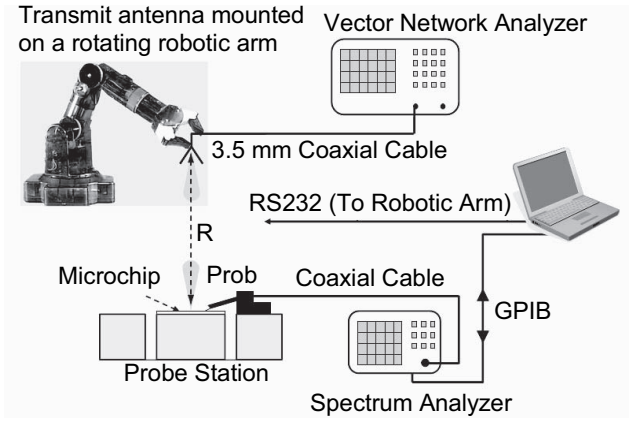

Fig. 5. On-wafer measurement setup used to measure the radiation pattern and radiation parameters of the miniaturized on-chip slot antenna.

III. Fabrication And Measuement

The on-chip antenna and its integrated LNA are fabricated in a 0.13µm RF CMOS process. Fig. 4 shows a microphotograph of the prototype I.C., including the 9 GHz miniaturized antenna and the LNA. The IC is die-bonded to a custom PCB which supplies power and DC bias. In order to assess the performance of the antenna, the measurement setup shown in Fig. 5 is used. A reference horn antenna operating at X-band is mounted on a rotating robotic arm. Both the antenna and LNA outputs are probed with high frequency GSG probes. A Vector Network Analyzer (VNA) is used to feed the horn antenna and the power received from the on-chip antenna is measured using a Spectrum Analyzer, as shown in Fig. 5. The distance between the reference horn antenna and the robotic arm is such that the two antennas are in the far fields of one another. Using this system, the radiation patterns of the antenna as well as its gain can be measured. The antenna, without the LNA, has a measured gain of -10dBi at 9GHz. The directivity of this electrically small antenna is almost identical to the directivity of an electrically small dipole (Hertzian dipole) antenna, which is about 1.76dBi. Therefore, using the relationship, η = Gain/Directivity, the radiation efficiency of this antenna is measured to be 9%. The LNA is designed to provide its maximum gain of 10dB at 9.5GHz. The maximum gain of the antenna-LNA combination is measured to be -4.4dBi. The measured gain of the active antenna and the antenna without LNA are both shown in Fig. 6. As is seen, the active antenna shows a higher measured gain in the 9-10 GHz frequency band of operation.

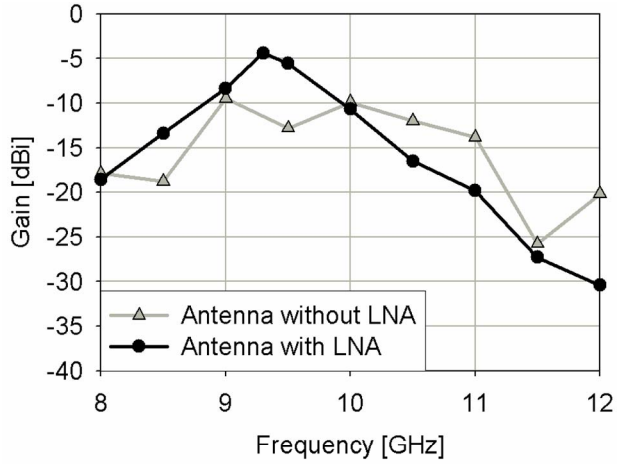

Fig. 6. Measured gain of the miniaturized on-chip slot antenna with and without LNA.

TABLE I
Comparison Between the Current Work and Those Reported In [1]-[2].

Antenna Type	Gain [dBi]	f_r [GHz]	Max. Linear Dimension
This work	-10.0	9.0	780 µm
Dipole Ant. [1]	-31.2	7.4	2000 µm
Zig Zag Ant. [2]	-17.0	15.0	2000 µm

To compare the performance of the current on-chip antenna with other state-of-the-art on-chip antennas reported in literature, one must keep in mind that a fair comparison is only possible when the frequency of operation and the maximum linear dimensions of the antennas are identical. For a fixed frequency, as maximum linear dimension decreases, the gain of the antenna also decreases [5]-[6]. Nevertheless, we attempt to make a fair

comparison between the current design and those presented in [1] and [2]. To do this, we use the associated gain definition, defined in [2] and used in [1]-[2] to extract the actual gain of the on-chip antennas presented in [1]-[2]. In doing so, we also consider the effect of mismatches between the antenna input impedance and the feeding source, since these effects have real implications in the performance of the antenna. This comparison is performed in Table I. As indicated by Chu, reducing the maximum linear dimension of any antenna significantly reduces its gain and radiation efficiency [5]. However, in spite of the smaller linear dimension of the on-chip antenna presented in this work, it demonstrates much higher measured radiation efficiency and gain values compared to those of the antennas presented in [1]-[2]. This can be attributed to the effective shielding of the antenna from the lossy silicon substrate, as well as the use of a slot topology instead of a wire-based approach such as the dipoles used in [1]-[2].

IV. CONCLUSION

A miniaturized on-chip antenna occupying a die area of only a $0.3mm^2$ was presented in this paper. This antenna is about 30 times smaller than traditional dipole or patch antennas operating at the same frequency. Furthermore, its direct integration with an on-chip LNA provides a higher effective gain. Utilizing a slot topology and an effective shielding technique to shield it from the lossy silicon substrate underneath, the antenna achieves a much higher gain and efficiency compared to other on-chip antennas, fabricated on low-resistivity silicon chips, reported in literature to date.

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