A Low Jitter Multi-Phase PLL with Capacitive Coupling

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***Abstract*-Capacitive coupling improves both phase noise and phase accuracy in coupled LC oscillators since the coupling current is in phase with the regeneration current. A prototype 3 GHz PLL with four LC oscillator stages and capacitive coupling is fabricated in 0.13μm CMOS. The long term measured RMS jitter of the buffered clock from the PLL is 1.61ps and the pk-pk jitter is 13.33ps.**

I. Introduction

In applications such as wire-line clock-and-data recovery, and RF down conversion, multiple clock phases are required. Traditionally, multiple clock phases are generated by rings of delay stages or with the help of interpolation, and in RF applications, poly-phase filtering is used to generate quadrature clock phases. Injection-locked rings of LC oscillators can also be used to generate multiple clock phases [1]. This approach is attractive, since in principle, coupling of LC oscillator stages can result in lower phase noise. Furthermore, coupling also reduces phase spacing errors caused by component mismatch [2].

In coupled, multi-stage LC oscillators, the out-of-phase coupling current from adjacent stages degrades the effective LC tank quality factor. Phase noise in a multi-stage oscillator typically depends on the phase difference between the coupling current and the regeneration current, while on the other hand, the error in phase spacing is related to the strength of the coupling signal [3]. In [3, 4] a phase shifter is introduced to minimize this phase difference and achieve low phase noise. A separate current source for the coupling differential pair is used in [3], to increase the coupling current and achieve low phase spacing error. We use a novel combination of conventional MOS transistor-based-coupling, and capacitive-coupling between stages, to achieve both low phase noise and accurate phase spacing [5]. Since in the case of capacitive coupling the phase of the coupling current is the same as the phase of the regeneration current, capacitive coupling does not degrade the effective quality factor of the LC tank.

II. PLL with Capacitively Coupled LC Oscillators

A simple two-stage coupled LC oscillator with conventional transistor-based coupling (solid line) and capacitive-coupling (dotted line) is shown in Fig. 1. In the figure starting at node 1, the sequence of the phases is in the order of nodes 1, 2, 1B, and 2B. Coupling capacitors are connected between adjacent phase nodes, such as between node 1 and 2 and between 2 and 1B. Capacitive coupling is introduced to increase coupling power,

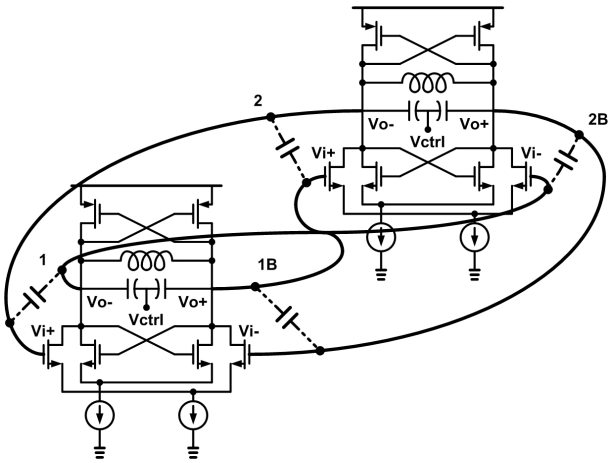

Fig. 1. Two-stage coupled LC oscillators with capacitive coupling

without increasing out of phase coupling current to each oscillator. Transistor-based coupling is used to force the correct oscillation mode and to set the direction of the phases. A four stage coupled oscillator is used in the prototype PLL.

A. Prototype PLL

Fig. 2 shows a block diagram of the prototype PLL. The four LC oscillator stages are coupled both with transistors (MN3 and MN4) and with capacitors (C1-C8). The coupling capacitors form a ring, connecting the oscillator nodes in the order of the phases; for example C1 connects the 0 and π/4 phase nodes and C2 connects the π/4 and π/2 phase nodes. Separate current sources are used to independently set the regeneration bias current for the cross-coupled transistors (i.e. generate negative resistance), and the bias current for the coupling transistors.

In this charge-pump PLL, the output signals from the oscillator stages are buffered and converted to full-swing, voltage signals. The frequency of one of the eight oscillator phases is divided by 32 and compared with the reference clock, *CLK*. *UP* and *DN* pulses from the phase frequency detector (PFD) control the charge pump. A 2nd order loop filter is implemented on-chip with MIM capacitors (CF1 is 60 pF and CF2 is 4 pF) and a poly resistor (R is 108 kΩ) to achieve a 1 MHz loop bandwidth. The frequency divider is implemented as five, divide-by-two blocks. The first two divisions are achieved with single-phase dynamic D flip-flops. The varactors are implemented as thin-oxide NMOS transistors in N-well.

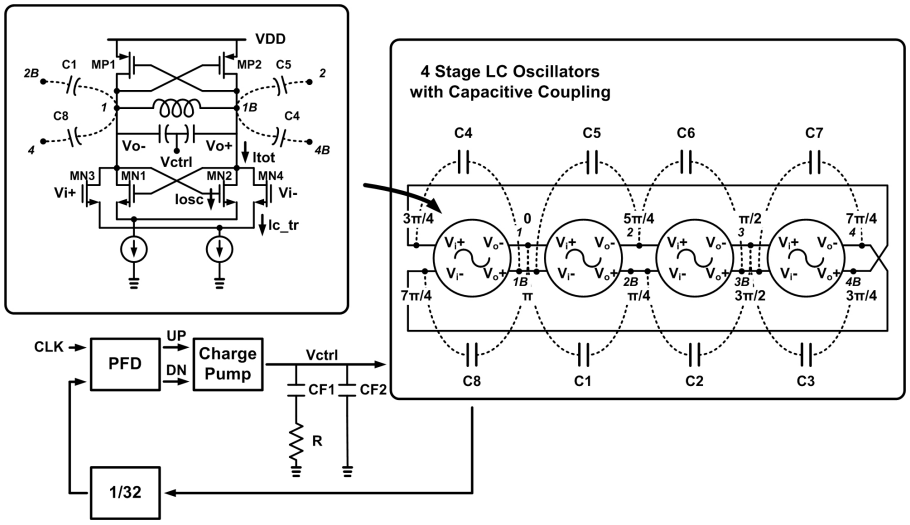

Fig. 2. Prototype PLL with capacitively coupled LC oscillator ring.

B. Phasor Diagram

A phasor diagram of a 4-stage, LC oscillator ring, with capacitive coupling is shown in Fig. 3. A ring of capacitors introduces another current path for injection locking of the LC oscillator stages. There are three current components at each oscillator node. For example, at node V_{o1}, the total current comprises of the regeneration current, I_{osc1}, and two coupling currents; the conventional transistor coupling current, I_{c_tr4b}, and the capacitor coupling current, I_{c_cap1}. Since one capacitor connects to an oscillator node 45 degree fast and the other to the node 45 degree slow, the total capacitor coupling current at V_{o1} (the sum of two components, I_{c_cap14b} and I_{c_cap12}), is in-phase with the regeneration current, I_{osc1}. The magnitude of the capacitor coupling current can much larger than the regeneration current I_{osc} at GHz operating frequencies. The current through the capacitors is proportional to the operating frequency, capacitance, and the phase across the capacitors. In the 3 GHz, 4 LC stage oscillator prototype, the simulated RMS current value through the 1 pF coupling capacitors is 10 mA. As shown in Fig. 3, thanks to the high, in-phase capacitor coupling current, the magnitude of the total coupling current, I_{tot1_cap}, is far larger than the case with conventional transistor coupling alone(I_{tot1_con}), resulting in improved phase accuracy. Furthermore, the phase difference between the total coupling current I_{tot1_cap} and the regenerative current I_{osc1} is far smaller than that between I_{tot1_con} and I_{osc1}, resulting in reduced phase noise. Even though the RMS current through each capacitor is large, the ring of capacitors does not require extra power, since sum of the currents in the ring is always zero.

C. Effective Capacitance

The coupling capacitors contribute to the tank capacitance in each stage, but this capacitive loading depends on the number of stages. Since the RMS current through each coupling capacitor depends on the voltage phase difference, θ, across the capacitor, then as the number of oscillator stages increases the RMS current decreases due to reduced phase difference. The coupling current through a capacitor of capacitance, C, connected between nodes at phase 0 and $-\theta$ is:

$$i = C\frac{d(V\cdot e^{j0} - V\cdot e^{-j\theta})}{dt}. \qquad (1)$$

From (1), the current flowing from the zero phase node to the $-\theta$ phase node can be represented as a current from zero phase node to ground, through an effective capacitance, $(e^{j0}-e^{-j\theta})\cdot C$. This effective capacitance contributes to the total tank capacitance. Therefore, considering this capacitive loading the operating frequency becomes:

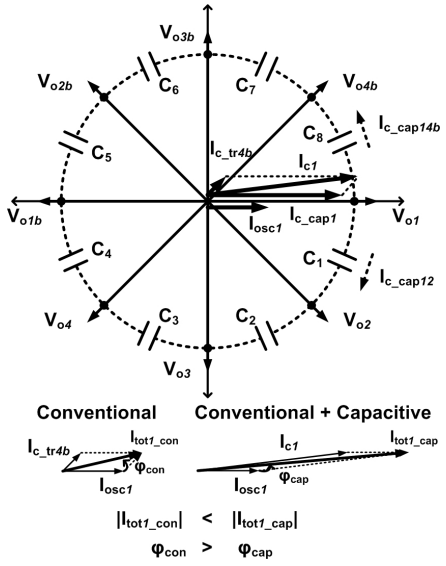

Fig. 3. Phasor diagram of 4 stage LC oscillator ring with capacitive coupling

$$\omega = \frac{1}{\sqrt{L \cdot \left(C_{tank} + \frac{\left| e^{j0} - e^{-j\theta} \right| \cdot C}{2} \right)}}. \quad (2)$$

Since the ring of capacitors acts as the fixed additional capacitance at each node, the tuning range of the LC tank may be decreased.

D. Modes of Operation

As we have seen, with the addition of capacitive coupling, two coupling methods (capacitive and transistor) work together in a multi-stage oscillator. A coupled oscillator, with capacitor-coupling alone, might exhibit several undesired modes of oscillation. For example, all of the oscillator stages might oscillate exactly in phase. Furthermore, when capacitive coupling is used alone, the direction of the oscillation is not defined. Therefore, capacitive coupling must always be used alongside transistor based coupling.

Fig. 4 shows coupling configurations, incorporating both conventional and capacitive coupling, that result in multiple oscillation phases for two, three and four stage coupled oscillators. Table I summarizes the modes of oscillation, indicating the phase difference between adjacent nodes for each mode. In the case of capacitive coupling, the fundamental mode (Mode 1) is the mode that dominates when the oscillator stages are coupled only with capacitors. Mode 2 is achieved when both capacitive and conventional couplings are used together. The required strength of the transistor based coupling depends on the number of stages. The use of separate current sources for the coupling transistor, as shown in Fig. 2, allows the control of the coupling power. Once oscillators begin operating in mode 2, they take advantage of the capacitive coupling, achieving lower phase noise and phase spacing error.

In case of four stages, coupled oscillators with capacitive coupling and with conventional coupling with transistors exhibit the same oscillator mode. In this case transistor coupling is only required to set the direction of oscillation and so can be very weak.

III. Experimental Results

A prototype PLL, die photo shown in Fig. 8, was fabricated in 0.13 μm CMOS. The PLL with 1 pF coupling capacitors, 2 mA regeneration current, and 1 mA transistor coupling current has a measured tuning range of 403 MHz, from 3.066 GHz to 3.469 GHz. When locked to a 108.4 MHz reference clock, and measured over a period of 25 minutes, the PLL achieves a long-term RMS jitter of 1.61 ps at 3.469 GHz, as shown in Fig. 5. The measured RMS and pk-pk jitter versus frequency is shown in Fig. 6(a) and (b) respectively. The total power consumption, including the power dissipated by the output buffer, is 32.5 mW, and total active area is 0.49 mm^2.

Fig. 7 compares the jitter and power dissipation of recently published CMOS LC PLLs[6-9] and this work. [6-8] measure RMS jitter by integrating the measured phase noise, from 10 kHz to 40 MHz, from 1 kHz to 10 MHz, and from 50 kHz to 80 MHz respectively.

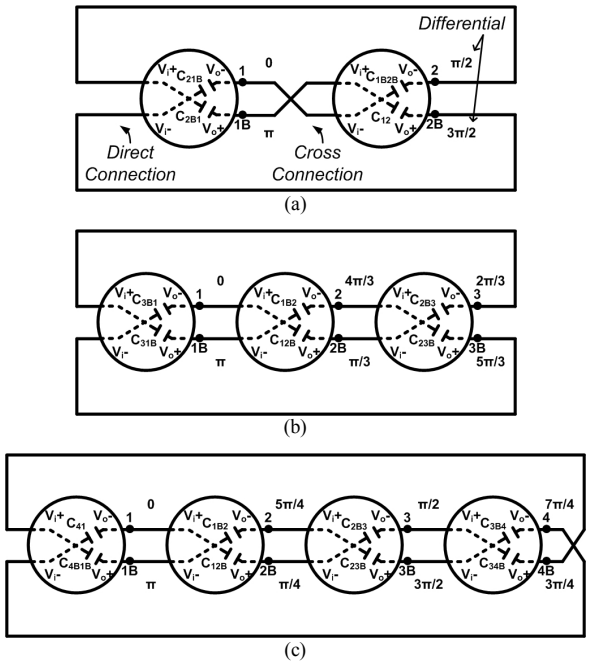

Fig. 4. Connections to generate multiple phases showing both capacitive coupling (dotted line) and conventional coupling with transistors (solid line); (a) Two stages, (b) Three stages, (c) Four stages

TABLE I
Modes of Operation, showing the spacing between phases.

Stage	Coupling	Modes	$\theta_{1\,2}$	$\theta_{2\,1B}$	$\theta_{1B\,2B}$	$\theta_{2B\,1}$
2	Conventional	1	**90°**	**90°**	**90°**	**90°**
	Capacitive	1	0°	180°	0°	180°
			180°	0°	180°	0°
		2	**90°**	**90°**	**90°**	**90°**

Stage	Coupling	Modes	$\theta_{1\,2B}$	$\theta_{2B\,3}$	$\theta_{3\,1B}$	$\theta_{1B\,2}$	$\theta_{2\,3B}$	$\theta_{3\,B1}$
3	Conventional	1	**60°**	**60°**	**60°**	**60°**	**60°**	**60°**
	Capacitive	1	180°	180°	180°	180°	180°	180°
		2	**60°**	**60°**	**60°**	**60°**	**60°**	**60°**

Stage	Coupling	Modes	$\theta_{1\,2B}$	$\theta_{2B\,3}$	$\theta_{3\,4B}$	$\theta_{4B\,1B}$	$\theta_{1B\,2}$	$\theta_{2\,3B}$	$\theta_{3B\,4}$	$\theta_{4\,1}$
4	Conventional	1	**45°**	**45°**	**45°**	**45°**	**45°**	**45°**	**45°**	**45°**
	Capacitive	1	**45°**	**45°**	**45°**	**45°**	**45°**	**45°**	**45°**	**45°**

IV. Conclusion

Capacitive coupling in a ring of LC oscillator stages reduces the phase difference between the coupling current and the regeneration current, improving phase noise and jitter performance. This capacitive coupling scheme can be extended to any number of stages, to provide accurate, finely-spaced clocks, for clock-and-data recovery and other applications.

If only capacitive couple is employed, there can be multiple modes, in case of two and three stage coupled oscillators, and therefore capacitive coupling is combined with transistor coupling to achieve the required multi-phase mode. In case of four stage coupled oscillators, both conventional transistor coupling and capacitive coupling produce the same mode, but weak transistor based coupling is still required, in addition to capacitive coupling, to set the direction of oscillation.

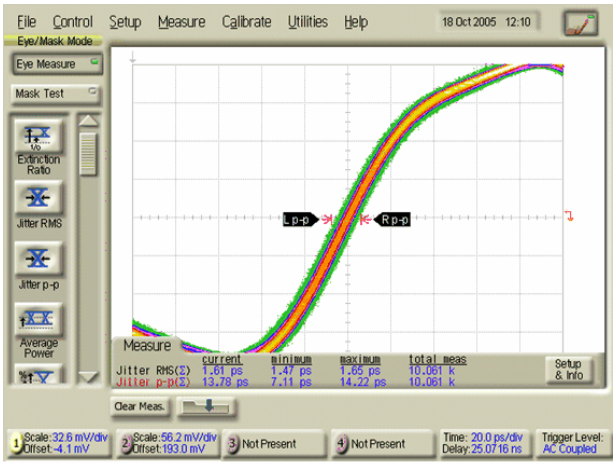

Fig. 5. 1.61 ps RMS jitter and 13.78 ps pk-pk jitter of the digital output of the PLL at 3.47 GHz

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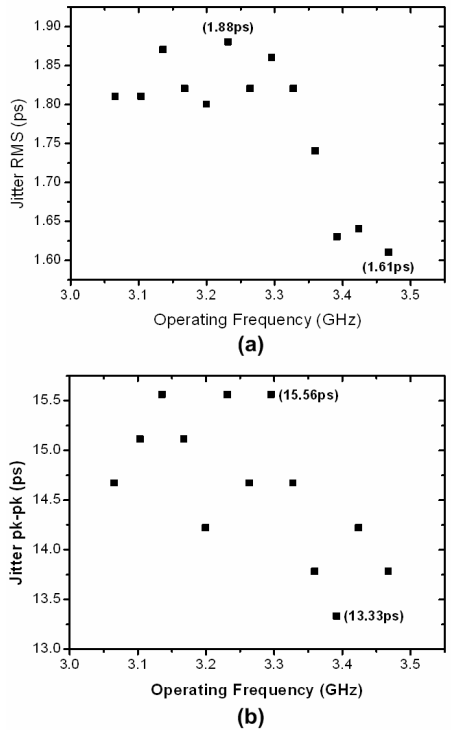

Fig. 6. (a)Measured RMS jitter and (b) measured pk-pk jitter

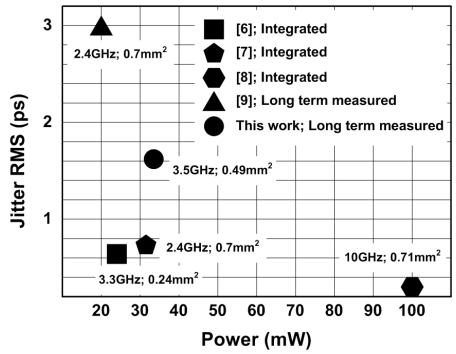

Fig 7. Jitter and power dissipation of published CMOS LC-PLLs and this work

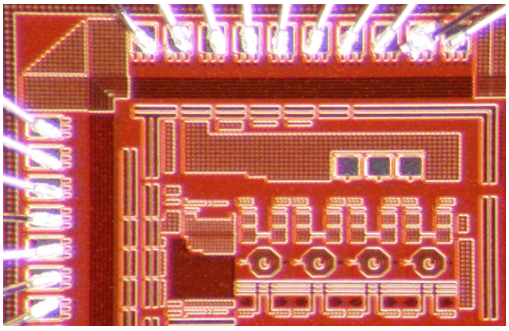

Fig. 8. Chip microphotograph of PLL