A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS

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***Abstract*—A 5-bit flash ADC incorporates 20 µm by 20 µm inductors to improve both comparator pre-amplification bandwidth and regeneration speed. A switched-cascode scheme reduces comparator kickback. Offset cancellation is achieved by modifying the comparator reference voltages without degrading high-speed performance. The ADC achieves a measured SNDR of 27.5 dB for a 5 MHz input at 4 GS/s, and 23.6 dB for a 1 GHz input at 3.5 GS/s. The power consumption (including clock buffer and ladder) is 227 mW at 3.5 GS/s. The active area is 0.658 mm^2.**

I. Introduction

Multi-GS/s analog-to-digital converters (ADC), with low resolution, are required in high-speed measurement systems [1], multi-Gbit/s wired communication receivers [2] and wideband wireless receivers (e.g. UWB). Time-interleaving of ADCs ([1], [2]) can extend the overall sampling rate, but time-interleaving requires precisely spaced, multi-phase clocks and accurate matching of ADC gain, offset and delay. Circuit techniques, that increase the sampling rate of a single ADC, for a given power consumption, are still fundamentally necessary.

We present a 1 GHz bandwidth, 3.5 GS/s 5 bit flash ADC prototype for UWB applications, implemented in 90 nm CMOS. We propose a modified comparator structure that outperforms our previous work [3]. We also propose a new offset cancellation scheme, based on programmable voltage buffers placed between the comparators and the resistor ladder. This scheme directly modifies the reference voltages to the comparators, but does not affect the high speed signal path.

II. High Speed Comparator

We show the comparator core in Fig. 1. The load is formed by the series combination of a resistor and an inductor. V_{INP} and V_{INM} are the differential analog inputs, V_{RP} and V_{RM} are the differential references voltages, and V_{OUTP} and V_{OUTM} are the comparator's outputs. When the complementary clocks, V_{CLKP} and V_{CLKM}, are low and high, respectively, the cross-coupled devices ($M_{7\text{-}8}$) are off, the input transistors ($M_{3\text{-}6}$) are enabled, and the comparator functions as a preamplifier. When V_{CLKP} and V_{CLKM} return high and low, respectively, $M_{7\text{-}8}$ are enabled and the comparator works as a regenerative latch.

Switched-cascode devices ($M_{1\text{-}2}$) reduce the parasitic capacitance at the latching node, improving the regenerative time constant. Additionally, the cascode devices significantly reduce kickback noise to the references inputs (V_{RP}, V_{RM}). The gates of the cascode devices ($M_{1\text{-}2}$) are controlled by the clock signal V_{CLKM}. Both the cascode devices ($M_{1\text{-}2}$) and switches $M_{9\text{-}10}$ are controlled by the same clock (V_{CLKM}). $M_{1\text{-}2}$ turn on later than $M_{9\text{-}10}$, since the source potential of $M_{1\text{-}2}$ is higher than that of $M_{9\text{-}10}$. Since $M_{1\text{-}2}$ turn on later, the residual charge from $M_{7\text{-}8}$ is dissipated through the output load (as V_{CLKP} goes low), and does not disturb the references.

The use of inductors in the comparator load (Fig. 1) not only increases the bandwidth in the pre-amplifier phase, but also improves the regeneration speed during the latching phase [3]. To minimize inductor area, we use a stacked, three-layer, differential inductor structure, implemented with a narrow metal trace (0.5 µm). The resulting 2.7 nH, seven turn differential inductor occupies only 20 µm by 20 µm. The inductor has a parasitic series resistance of 144 Ω, and this contributes to part of the total load resistance. The optimum inductance depends on the parasitic capacitance, so that a smaller inductance is required in more advanced CMOS processes [4]. In this 90 nm CMOS prototype, the inductor area is 2.56 times smaller than that in [3] (0.18 µm CMOS).

For faster switching, we use a clock amplitude less than the supply voltage. Since all of the switches in the comparator core are implemented as NMOS devices, the on/off threshold is set closer to V_{DD} than ground. With faster clock switching, for a given sampling frequency, more time can be spent on regeneration. Fig. 2 compares the simulated comparator core output waveforms with a full swing clock (1.4V) and a reduced swing clock (0.9V), assuming the same rise and fall times. In this comparison, we see that we gain an additional

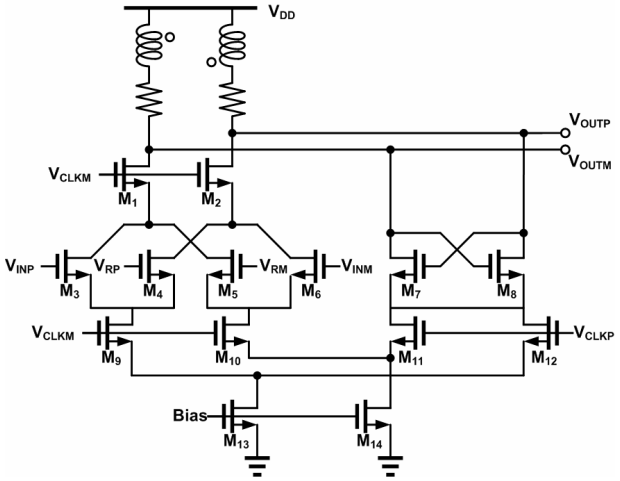


Fig. 1. Comparator core.

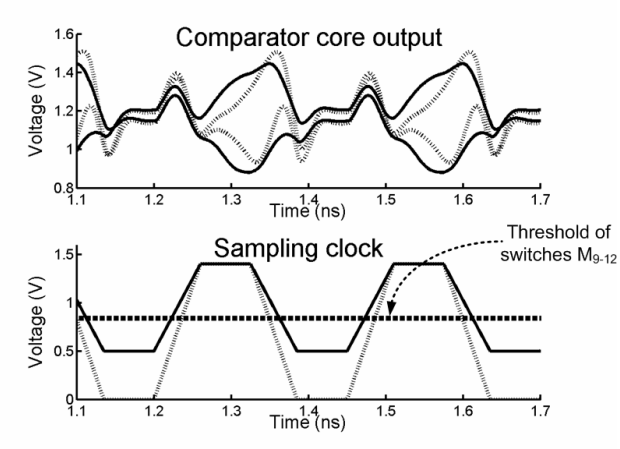


Fig. 2. Comparator core output waveforms with different clock amplitude (0.9 V and 1.4 V).

32 ps for regeneration with the 0.9 V clock swing, even though the 0.9V swing clock, in this example, has a lower slew rate.

Fig. 3 (a) shows the entire comparator unit comprising of the comparator core (Fig. 1), a latch, and a D flip-flop (D-FF). Fig. 3 (b) shows the timing diagram of the entire comparator unit. Fig. 4 (a) shows a schematic of the latch ([5]) that follows the comparator core. The latch provides additional gain, further reducing the probability of the metastability. Fig. 4 (b) shows a schematic of the D-FF. A differential static D-FF is used. A static flip-flop design enables the ADC to operate properly at both low and high sampling frequencies, unlike the case with some dynamic flips-flops. The back-to-back inverter structure in the D-FF provides additional regenerative gain, further reducing the risk of metastability.

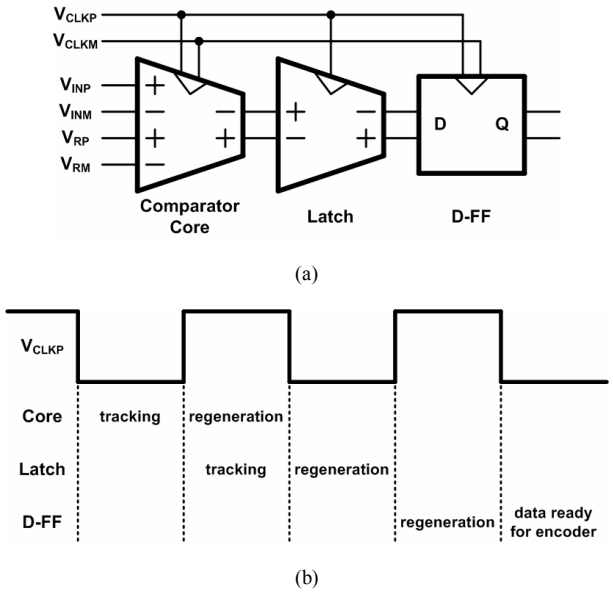


Fig. 3. Comparator unit with timing diagram.
(a) Comparator unit. (b) Timing diagram.

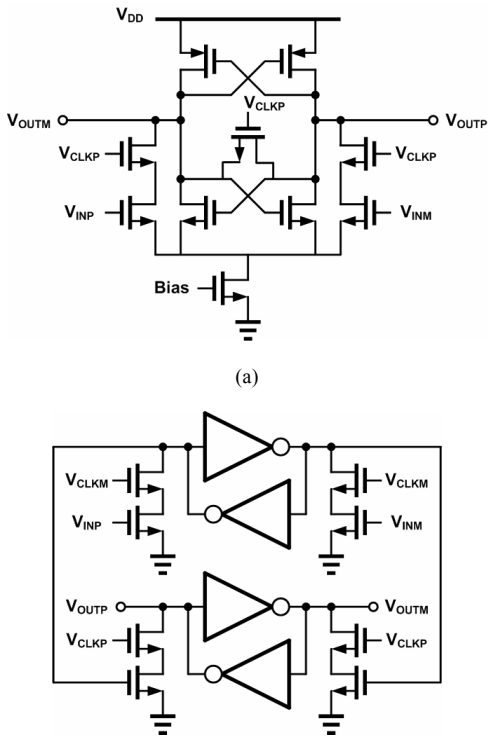


Fig. 4. Schematics of latch and D flip-flop.
(a) Latch. (b) D flip-flop.

III. Comparator Offset Calibration

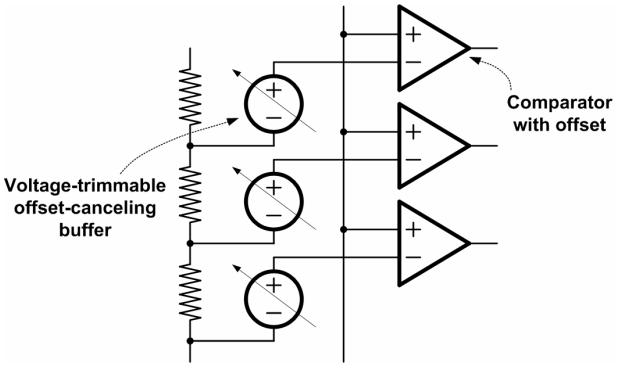
Fig. 5 (a) shows part of the flash ADC, that explains the proposed offset cancellation system. The differential reference voltages to each comparator pass through a voltage-trimmable offset-canceling buffer. Fig. 5 (b) shows a schematic of the offset canceling buffer. V_P and V_M are DC voltages from the metal-resistor reference ladder, and V_{RP} and V_{RM} are the reference voltages passed to the comparator core (Fig. 1). This buffer is essentially a source follower. Two current sources, and the differential current from a 16 level, thermometer-coded digital-to-analog converter (DAC), supply the biases for the source followers. If there is no comparator offset, the DAC is set to provide a differential current of zero, giving an equal level shift to both halves of the differential reference.

When the calibration starts, we (externally) set the differential analog input to zero. We also provide a zero differential reference voltage by shorting the gates of M_{IN} in Fig. 5 (b) (the gates of M_{CAS2} are also shorted). Therefore, the digital output of the comparator is determined only by the comparator offset and the source follower offset.[1] To calibrate a comparator offset, the DAC calibration logic first steers the entire DAC current in one direction. The current DAC is

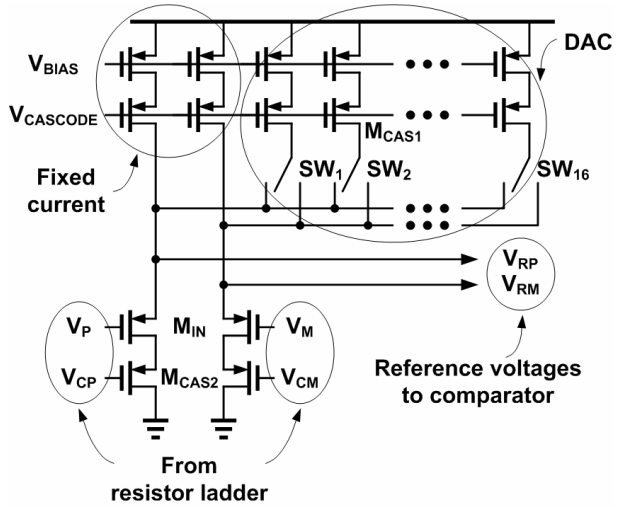
[1] Both comparator and source follower offsets are corrected.

decremented in 1 LSB steps until the comparator's digital output changes (i.e. the comparator offset is minimized.). The DAC search is based on the comparator's digital output, and the comparators run at the full sampling rate during calibration. Therefore, this calibration corrects both static and dynamic offsets. This scheme corrects comparator input offsets, of up to ± 3.5 LSB, to an accuracy of 0.44 LSB. The DAC clock frequency is 64 times slower than the ADC sampling clock to ensure sufficient DAC settling. The DAC LSB size is 3.3 µA. Each offset-canceling-buffer consumes 64 µW.

The DAC current sources are cascoded (M_{CAS1}) to maintain a constant DAC current over a wide reference voltage range. The input devices M_{IN} are also cascoded (M_{CAS2}). For a given bias current, M_{CAS2} keeps the drain-source voltage of M_{IN} constant, and therefore V_{GS} of M_{IN} does not change for various values of reference voltages V_P and V_M. Since V_{GS} of M_{IN} are kept constant, regardless of the gate voltage V_G of M_{IN}, the comparator offset is corrected during normal operation. The gate voltages V_{CP} and V_{CM} are also derived from the resistor ladder, with $V_P - V_{CP}$ and $V_M - V_{CM}$ set to be the same for all reference voltages. Fig. 6 shows how we implement the resistor ladder that generates the reference voltages V_P, V_M, V_{CP}, and V_{CM} of Fig. 5 (b). All MOS bodies are tied to their sources to remove the body effect on the threshold voltage.



(a)



(b)

Fig. 5. Offset canceling scheme.
(a) Buffers, comparators and resistor string (shown as a single-ended configuration for simplicity). (b) Buffer schematic.

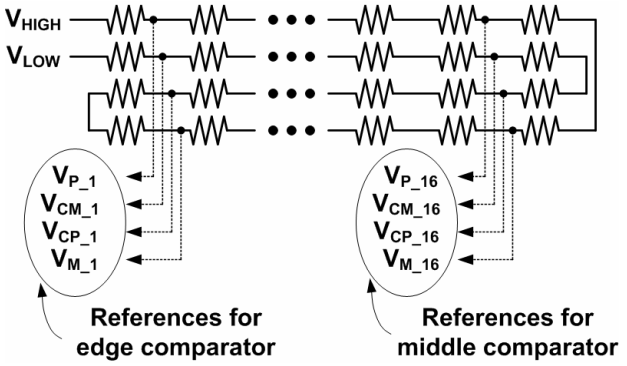


Fig. 6. Resistor ladder implementation.

The reference buffer only affects the DC reference voltage path, and is not connected directly to the comparator's high-speed signal nodes. In this way both accuracy and speed can be achieved simultaneously. In simulations, the voltage difference $V_{RP} - V_{RM}$ varies by less than 0.35 LSB over all process corners and over a temperature range from 25 to 85 degrees Celsius.

IV. ADC Structure

Fig. 7 shows the 5-bit flash ADC. It contains thirty one comparator units (a unit shown in Fig. 3 (a)) each with an accompanying offset-canceling buffer, the resistor ladder (shown in Fig. 6), a thermometer-to-binary encoder with three-input NAND gate for transition detection, Gray-code bubble/sparkle correction, offset correction logic, and clock buffer. The differential analog input (*Input* in the figure) is directly connected to two input pads without a track-and-hold to save power consumption.[2] The clock buffer generates the

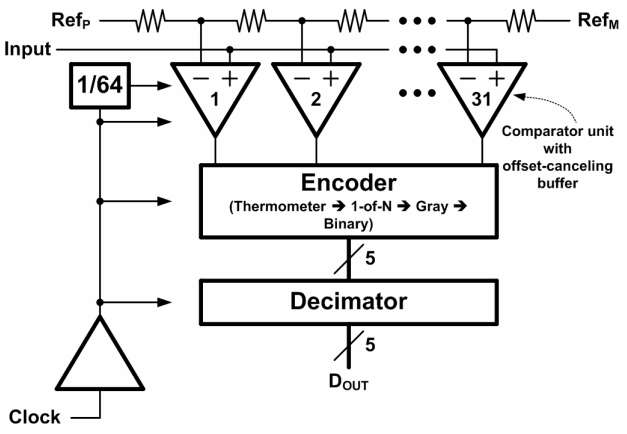


Fig. 7. ADC architecture.
(Offset correction logic not shown for simplicity)

[2]The clock and analog input are distributed in a symmetrical tree structure to minimize the skew.

high-frequency clock for the comparators and the encoder, and the (decimated) low-frequency clock for the DACs of the offset-canceling buffers. The ADC decimates the 5-bit digital output by 64 to facilitate characterization of the prototype.

V. Measurement Results

The ADC, micrograph shown in Fig. 8, is implemented in 90 nm Intel CMOS. A bare-die was mounted on a PCB and wire-bonded for characterization. Fig. 9 shows the measured DNL and INL, measured at 3.5 GS/s with a 5 MHz input frequency, before and after calibration. We see that the proposed offset calibration technique improves the ADC linearity. Fig. 10 shows the measured SNDR vs. sampling frequency for 5 MHz and 1 GHz input frequencies, before and after calibration. We see that, after the calibration, the SNDR remains relatively constant as we increase the frequencies of the sampling clock and the analog input. We note that, at 3.5 GS/s with 1 GHz input frequency, SNDR improved by 22.8 dB after the calibration. We summarize the ADC performance in Table I.

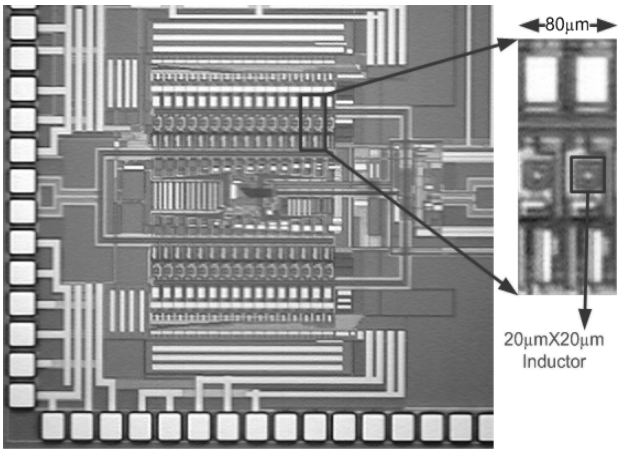


Fig. 8. ADC micrograph, with a magnified view of two comparators.

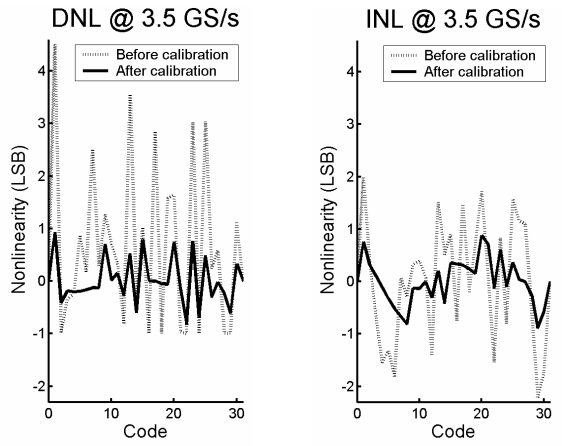


Fig. 9. DNL and INL at 3.5 GS/s.

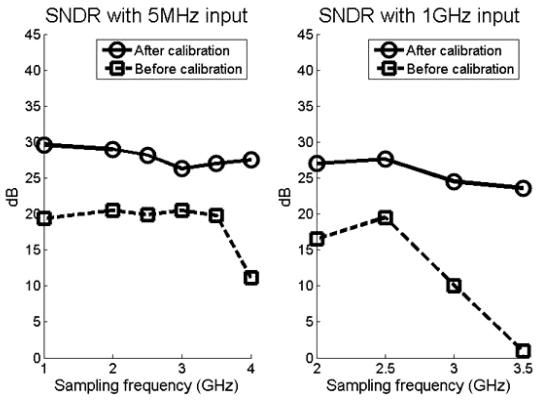


Fig. 10. SNDR with 5MHz and 1GHz input frequencies.

TABLE I
ADC Performance

Technology	CMOS 90 nm
Resolution	5 bits
Supply	1.4 V analog, 1.4 V digital, 1.8 V clock buffer
Input range	± 320 mV (LSB = 20 mV)
Sampling rate	Up to 4 GS/s
Power	227 mW (115 mW: comparators, resistor ladder, bias. 17 mW: D-FFs, encoder, decimator. 95 mW: clock buffer)
DNL @ 3.5 GS/s	-0.83 LSB ~ 0.93 LSB (after calibration) -1.00 LSB ~ 4.51 LSB (before calibration)
INL @ 3.5 GS/s	-0.89 LSB ~ 0.88 LSB (after calibration) -2.20 LSB ~ 1.98 LSB (before calibration)
SNDR	27.5 dB @ 4.0 GS/s, 5 MHz input 23.6 dB @ 3.5 GS/s, 1 GHz input
Active area	0.658 mm^2 (including resistor ladder)
Input capacitance	540 fF
Package	Bare-die on board

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