A New Transponder Architecture With On-Chip ADC for Long-Range Telemetry Applications

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***Abstract*—We present a new architecture for wireless power and data telemetry that recovers power and a system clock from a weak incident RF signal. A high-efficiency RF–DC converter generates a 3-V_{DC} supply for the system from a −12.3-dBm incident RF signal, gathered by a commercial 50-Ω antenna. A system clock is extracted from the same incident signal, by an injection-locked LC oscillator. Sub-harmonic injection-locking facilitates the separation of the incident and the transmit signal frequencies, without need for a PLL. The proposed architecture is used in a long-range telemetry device, incorporating an on-chip ADC, and employing active telemetry for data transmission. Data is transmitted through binary phase-shift-keying of a 900-MHz carrier. The prototype, implemented in 0.25-μm CMOS, occupies less than 1 mm^2. A wireless operation range of more than 18 meters is indicated by anechoic chamber testing.**

***Index Terms*—Active telemetry, injection-locked oscillator, passive RFID, power telemetry, RF–DC conversion.**

I. Introduction

WIRELESS data telemetry and wireless power transfer are used in radio frequency identification devices (RFID) [1] and implanted biomedical devices [2], [3]. The application areas are diverse, including access control, highway toll collection, personnel identification, vehicle theft detection, manufacturing control, and patient monitoring. The performance of these systems is also diverse due to differing requirements in various applications. Implanted biomedical devices and contactless entry devices can be in close proximity (∼10–50 cm) to a base station. On the other hand, longer range operation (∼1–2 meters) is desirable for applications such as warehouse navigation, manufacturing control and remote access control. In such cases, ultra-high-frequency (UHF) transponders are usually employed, and these work in the far field of the base station. For applications demanding very long operational range, battery-assisted systems are used, achieving a range of operation of over 30 meters.

Recently, there has been a growing interest in the integration of sensing and telemetry to create smart tags and sensor networks [4]. These systems require long-range operation (preferably above 10 meters) and batteryless operation for low cost. In such sensor networks, high data rate transmission is desirable to achieve low duty-cycle operation, so that the system can *sleep* most of the time. Some biomedical applications such as neural recording [5] also require high data transmission rates (∼2 Mb/s).

Passive tags reported in the literature have an operating range of less than 10 meters. The device in [6] employs a Schottky-diode-based rectifier and achieves a range of 9.25 meters. However, the use of a nonstandard CMOS process incorporating Schottky diodes prevents this design from being implemented in most standard foundry processes, which increases cost. Moreover, the backscattering-based data transmission technique used limits the data rate of the device.

In this paper, we present a new transponder architecture for long-range high data rate communication. The system presented is fully compatible with CMOS. Section II gives a detailed description of the proposed architecture. A CMOS compatible RF–DC converter generates a useful supply voltage from a very low incident RF power. An on-chip mode selector continuously monitors the generated supply voltage and keeps the system in a standby mode until sufficient energy is gathered by the RF–DC converter to operate the device. When enabled, a 5-bit analog-to-digital converter (ADC) generates 5 bits of an 8-bit transmit data word. The remaining three bits are programmed externally as the ID-tag of the device. The transponder then transmits this 8-bit data on a binary phase-shift keying (BPSK) modulated 900-MHz carrier. An on-chip power amplifier drives a 50-Ω transmit antenna.

II. System Overview

Traditionally, most telemetry devices employ a voltage rectifier with one or two diodes and a large capacitor to generate the DC supply voltage for the system. This voltage doubler rectifies the incoming RF signal and generates a constant DC voltage for the rest of the system blocks. It should be noted that the DC supply voltage stored on the capacitor cannot exceed the peak-to-peak amplitude of the received RF signal. Therefore, the magnitude of the incident RF signal must be large to guarantee the functionality of the system. This may require the power sent by the base station to be near the maximum set by FCC regulations, and limits the distance between the wireless device and the base station.

A block diagram of the proposed architecture is shown in Fig. 1 [7]. We employ a new architecture for efficient RF-to-DC conversion. The converter generates useful DC supply voltage even with very low RF signal amplitudes. This telemetry IC accumulates energy in *charging* mode, increasing the range

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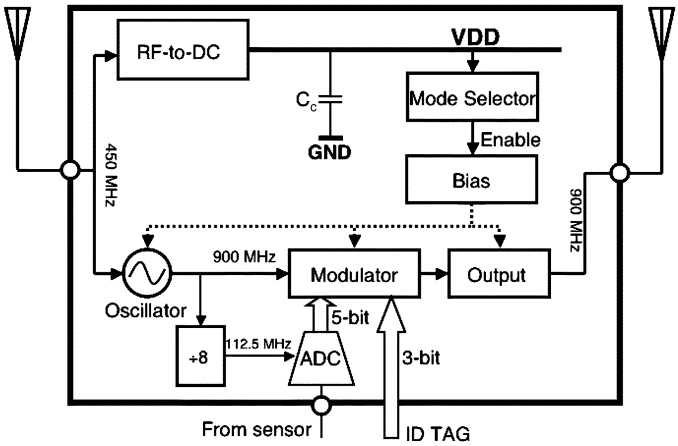

Fig. 1. Block diagram of the proposed architecture.

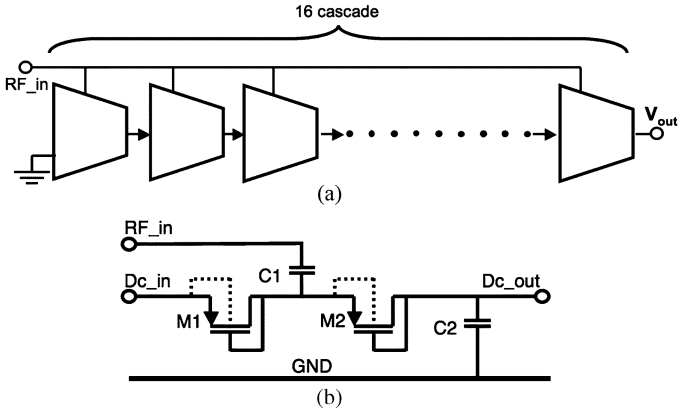

Fig. 2. RF–DC converter. (a) Block diagram. (b) Schematic of a single stage.

from the base station and reducing base transmit power. A mode selector circuit detects when the capacitor voltage exceeds a threshold (3 V), powering up the data telemetry circuitry. The system continues to operate until the capacitor voltage drops below a lower threshold (1.5 V). At this point, the telemetry circuit is powered down, allowing the capacitor to recharge. This dual mode operation allows useful energy to be scavenged from a weak incident RF signal; however, given a sufficiently high received power level, the telemetry circuit can operate continuously.

We present a new clock recovery circuit, which employs a fully integrated injection-locked LC oscillator. The oscillator is designed for minimum power dissipation with a measured supply current of only 650 μA. In conventional systems, a system clock is extracted from the incident RF signal, usually with the help of a Schmitt trigger, coupled directly to the antenna or receiving coil. The clock generated by the Schmitt trigger has high phase noise which limits transmission rates, especially when the RF signal received is weak—for example in long-range applications. Schmitt triggers also are prone to jitter due to supply voltage variation and ripple, both of which are significant in batteryless devices. Moreover, this method generates a clock frequency equal to the incident signal frequency. A power-hungry PLL may be required to ensure that the transmitter of the device operates at a different frequency to prevent collision.

A key feature of this approach (unlike other designs [8]) is that there is no on-chip supply regulation. Simple regulators, such as source followers, are inefficient and require a relatively accurate reference voltage from a zener or bandgap reference. Instead, by tolerating large variations in supply voltage, we can efficiently discharge and utilize the energy stored on the capacitor. On the other hand, all system blocks must now operate over a large supply range (3–1.5 V) and with low supply sensitivity. As we will see, all circuit blocks are designed to work with low supply voltages ($<$1 V) and with low supply sensitivities. For a given capacitor size and receive power, the duration of active operation and the duty cycle of the system are determined by the total power consumption. Therefore, all circuitry is designed for minimum power dissipation.

The on-chip LC oscillator generates the system clock and the RF carrier. The LC oscillator is injection-locked to an integer fraction of the incident RF signal. A BPSK modulator and a power amplifier (PA) working in the class-B regime modulate the transmit data onto a 900-MHz carrier. The low-frequency modulation signal is synchronously generated by dividing the low-phase-noise 900-MHz system clock. We now discuss the system blocks in detail.

A. RF-to-DC Converter

A CMOS implementation of the Cockcroft–Walton multiplier circuit [9], with 16 cascaded stages, generates a DC voltage higher than the peak incident signal amplitude. A block diagram of the converter and schematic of a single stage are given in Fig. 2. Each stage has two inputs, the DC output voltage from the previous stage and the RF input from the receiving antenna. Each stage works as a voltage rectifier adding the peak RF voltage to its DC input voltage. Diodes are implemented as diode-connected low $V_{\rm TH}$ PMOS transistors, to achieve low-voltage operation and reduce energy loss. The voltage drop across each diode-connected transistor is only 150 mV at 17 μA. With this circuit, for an input signal amplitude of only 150 $\mathrm{mV_{rms}}$ (210 $\mathrm{mV_{peak}}$), 3 $\mathrm{V_{DC}}$ is generated.

With a 1-MΩ load resistor and an input power of 63.1 μW at 450 MHz, the measured output power is measured as 6.9084 μW, which corresponds to a power efficiency of 10.94%. For comparison, the reported efficiency of the rectifier in [6], which employs specially designed Schottky diodes with low resistance and capacitance, is 14.5%. Wireless tests of the RF-to-DC converter were performed in a 2-meter-long anechoic chamber. The measured input impedance at 450 MHz of the system has a small resistive component ($\sim$ 12 Ω) and a small reactive part ($\sim -10\ \Omega$) (which corresponds to 50 pF). A microstrip line-matching board matches the input impedance of the system to that of a 50-Ω antenna. Fig. 3 shows the test PCB and the matching board during anechoic chamber tests. With the telemetry device placed 1.65 meters from the transmitter, the minimum RF power transmitted from the base station to generate a 3-$\mathrm{V_{DC}}$ supply was measured as 17.5 dBm ($\sim$55 mW). Using Friis' free space propagation formula [10], this corresponds to a maximum operating distance of 18.3 meters (for a 3-$\mathrm{V_{DC}}$ output) with the 7-W

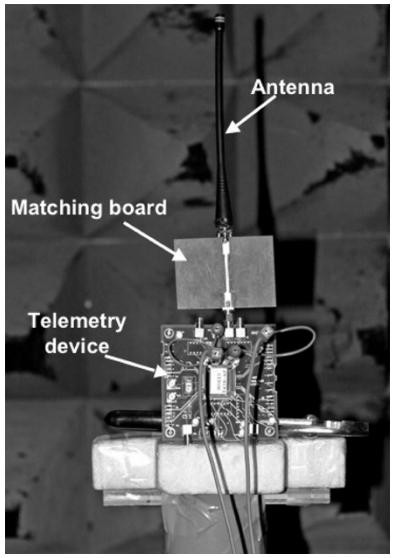

Fig. 3. Wireless testing in an anechoic chamber.

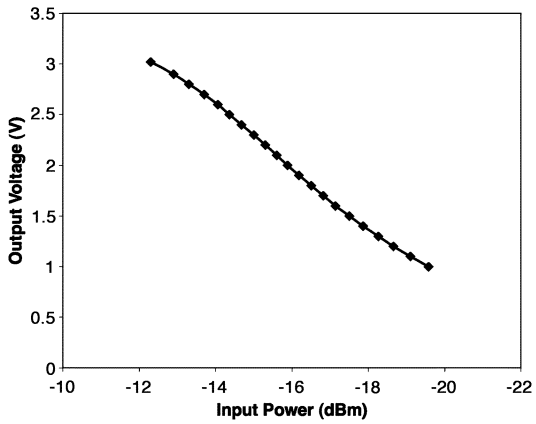

Fig. 4. Measured generated DC voltage versus input power.

(38.5-dBm) maximum transmit power from the base station. With the minimum required storage capacitor of 4 nF, it takes approximately 600 μs for the system to generate 3-V_{DC} output. The measured generated supply voltage scales linearly with the incident RF power, as shown in Fig. 4. To generate 1 V_{DC}, only -19.58 dBm of incident RF power is required.

B. Mode Selector and Bias Generator

The mode selector circuit monitors the supply voltage and decides whether the system is in charging mode or enabled. In charging mode, the system waits while the capacitor charges and dissipates very little current. The system is enabled when the voltage stored on the storage capacitor exceeds 3 V. Enabled, the system draws current from the capacitor, discharging it. The system returns to standby mode when the voltage on the storage capacitor drops below 1.5 V. During the charging phase, only the mode selector is active. This block dissipates less than 900 nA.

The mode selector is shown in Fig. 5. Two trip voltages are generated by two resistive ladders and compared by a hysteresis comparator formed with transistors M1–M6 [11]. A common-source amplifier (M13 and M20) buffered with a current starved inverter (M14, M15, and M21) generates the output enable logic signal. These buffers make the transition between logical output levels fast, yet dissipate little current. The quiescent bias of the comparator, amplifier, and the current-starved inverter is set by the transistor chain M16–M18.

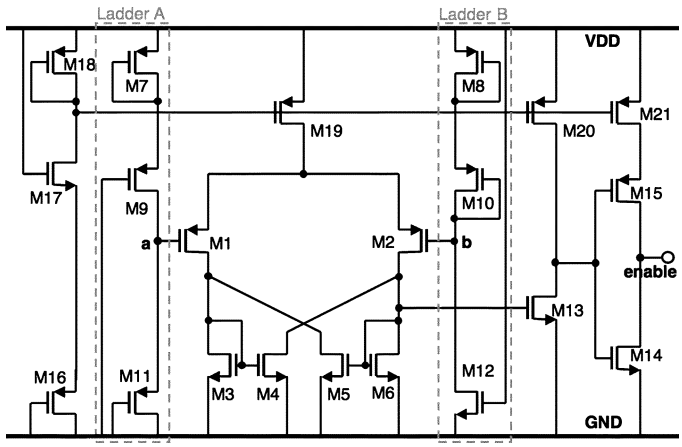

Fig. 5. Schematic of the mode selector.

It should be noted that the bias current of the comparator changes with changing supply voltage. Therefore, the logical output changes from low to high when the difference between the two comparison points is 960 mV, and high to low when the difference is -170 mV. The resistor ladders are adjusted to accommodate this variation. Diode-connected transistors M7, M8, M10, and M11, implemented as high-V_T transistors, turn off the ladders when V_{DD} is less than 1.5 V, further decreasing power consumption.

The bias generator, shown in Fig. 6, provides a stable bias for the oscillator and other circuits, yet dissipates only 24 μA. Transistor switch M6, controlled by the mode selector, enables the bias generator. In this bootstrapped bias generator, the voltage drop across resistor R_s equals the gate–source voltage of transistor M3, setting the bias current as given in (1):

$$I_{\text{gen}} = \frac{V_{\text{GS-M3}}}{R_s} \tag{1}$$

where I_{gen} is the bias current generated and $V_{\text{GS-M3}}$ is the gate–source voltage of M_3. Since the generated current depends directly on the value of resistor R_s, we use polysilicon resistors, the most accurate resistors provided in a conventional CMOS process. Since the sheet resistance of polysilicon is small, we implement M3 as a medium threshold device in order to generate a low bias current (12 μA) with a relatively small resistor (20 kΩ.) The bias output voltages *bias* and *div_bias* are used by other blocks.

Since the enable high-voltage tracks the V_{DD} during active operation (i.e., while enable is high), the on-resistance of M6 varies significantly during operation. A dummy switch M5, inserted between the source of M3 and ground, compensates for the varying voltage drop across switch M6. The addition of M5 decreases the supply dependence of the bias generator by a factor of four.

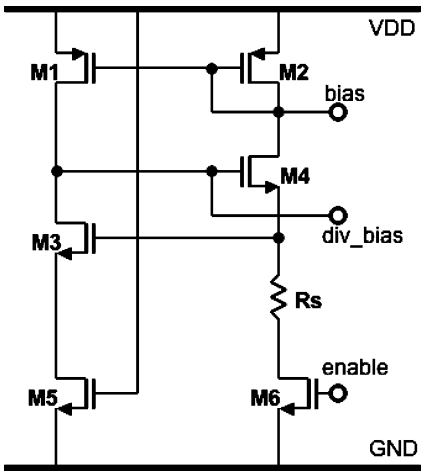

Fig. 6. Schematic of the bias generator.

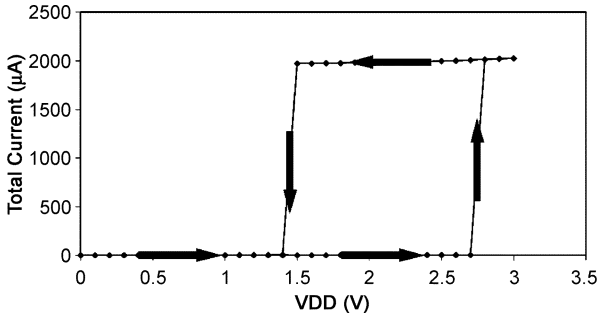

Fig. 7. Measured IC supply current under DC sweep of the supply.

The functionality of the mode selection is tested by sweeping the $V_{\rm DD}$ supply between 0 and 2.6 V and measuring the total current consumption of the system. The measured current consumption of the entire IC is plotted in Fig. 7. The measured hysteresis curve clearly shows the operation of the mode selector and bias generator.

C. Injection-Locking and Clock Generation

Traditionally, a Schmitt trigger circuit is used to extract the system clock. The phase noise of the clock generated by this method is high, especially when the incident signal strength is small, limiting use to low data rate applications. We present a new approach for on-chip clock generation, where a reference clock is extracted from the incident RF signal using an injection-locked oscillator [12]. Injection-locking is far more power efficient than a Schmitt trigger or a PLL scheme, and delivers a recovered clock with very low phase noise and phase jitter. By locking to a harmonic of the incident signal, frequency separation between the incident signal and the transmitted carrier is achieved without using a PLL. A low-power LC oscillator, shown in Fig. 8, lies at the heart of the injection-locking scheme. The LC oscillator is biased with a cascoded current source (M3 and M4) to decrease the supply dependence of the oscillation frequency. M5–M7 generate the bias voltage for the cascode transistor M4. The oscillation frequency of the LC oscillator is

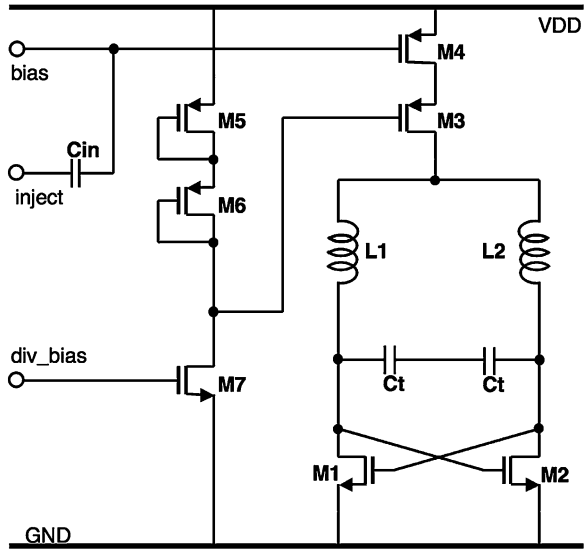

Fig. 8. Schematic of the injection-locked LC oscillator (ILO).

determined by the tank capacitance and inductance values and is given by

$$\omega = \frac{1}{\sqrt{L_s C_t}} \tag{2}$$

where ω is the oscillation frequency in radians per second, L_s is the equivalent inductance and C_t is the equivalent tank capacitance. C_t is formed with a 32-segment trimmable- capacitor array. The frequency of oscillation is adjusted by laser trimming.

The oscillator frequency, however, can be locked to an injected signal close in frequency to the free running frequency of the oscillator. In an LC oscillator, the injected signal can be applied to a high impedance node such as the bias branch, labeled as the *inject* port in the figure. It is possible to lock to a sub-harmonic [13] or a super-harmonic signal [14] of the injected signal. The locking range of the oscillator depends on the locking signal strength. We achieved a measured locking range of 12 MHz when locking a 900-MHz LC oscillator to a 450-MHz 140-$\rm mV_{rms}$ incident signal. A plot of showing superimposed measured outputs of the oscillator, locked at three extremes, is shown in Fig. 9.

For low-voltage operation, the oscillator uses only NMOS cross-coupled devices (M7, M8). The oscillator is operated in current limited mode to minimize power dissipation. The effective parallel resistance R_p of an LC tank is given by

$$R_p = \frac{L_s}{C_t \times R_s} \tag{3}$$

where L_s is the tank inductance, C_t is the tank capacitance, and R_s is the series resistance of the inductor L_s. For low power consumption, the effective parallel resistance must be large. Since the series resistance of a planar inductor increases linearly with the inductance [15], we achieve maximum effective tank resistance by maximizing inductance. (For a given oscillation frequency, any increase on the inductance requires a decrease of

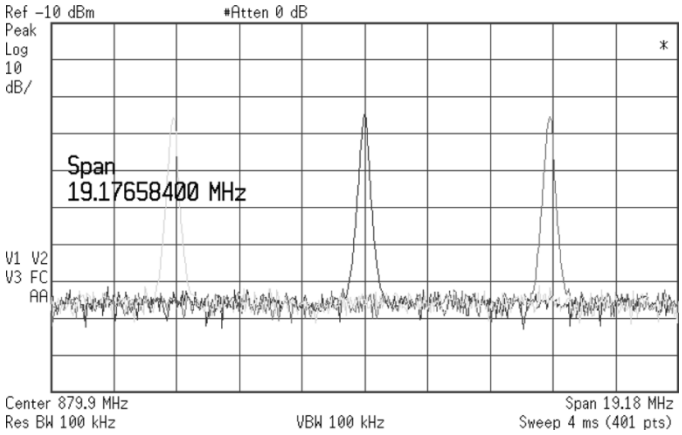

Fig. 9. Oscillator output spectrum when injection-locked to three extremes.

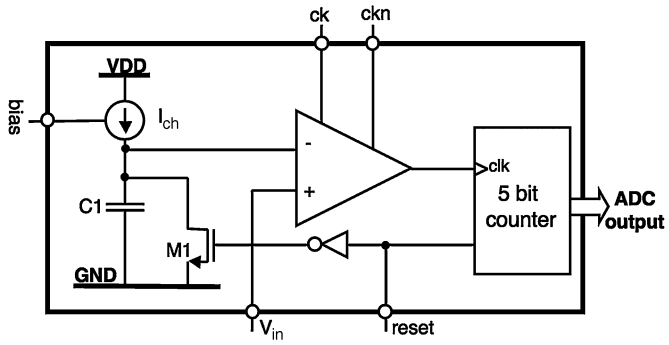

Fig. 10. Block diagram of the ADC.

the tank capacitance.) In this way, the current dissipation of the oscillator is reduced to 650 μA.

Thanks to the nature of LC oscillators, the system shows very good phase noise performance. The measured phase noise of a free running oscillator (no injection lock) is -94 dBc/Hz at an offset of 100 kHz. The measured phase noise drops to -113 dBc/Hz when the oscillator is locked to the $f/2$ harmonic. The free-running oscillator has a figure of merit (FOM), as defined in [16], of 175 dBc/Hz. The FOM improves to 185 dBc/Hz when the oscillator is locked to the $f/2$ subharmonic and to 192 dBc/Hz when locked to the $2f$ superharmonic. The measured FOM is close to the state of the art [17].

D. Single-Slope ADC

A block diagram of the single-slope on-chip ADC is shown in Fig. 10. A single-slope architecture is employed because of its simplicity. Moreover, since it only needs a single comparator, it occupies a very small area.

A high-output resistance current-source charges an integrating capacitor, while the capacitor voltage is compared with the input voltage to the ADC $(V_{\rm in})$. The comparator decision remains at 1 while the capacitor voltage is less than the input voltage. After each comparison, the comparator resets and its output returns to zero. In this way, the comparator output forms a clock signal while the capacitor voltage is less than the input voltage. This clock increments a counter while the capacitor voltage is less than the input. Both the reference current and reference voltage are supplied by the on-chip bias generator.

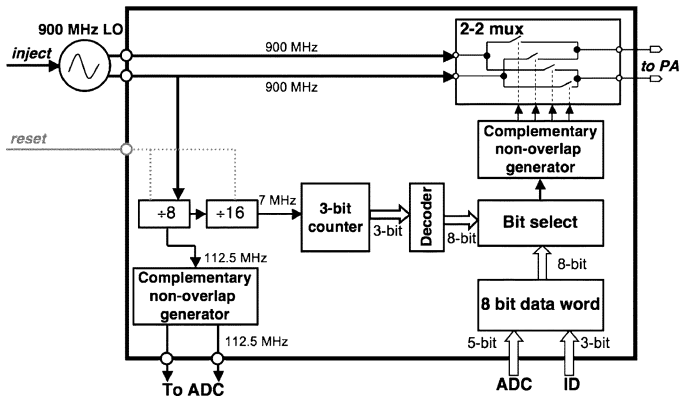

Fig. 11. Block diagram of the BPSK modulator.

The ADC is enabled and disabled along with other system blocks.

E. Modulator

The IC incorporates a compact yet power-efficient BPSK modulator, shown in Fig. 11. A divide-by-128 generates a synchronous 7-MHz clock for the modulator. This approach differs from most modulator architectures where a lower frequency is already available. True single-phase D-flip-flops (DFFs) [18] are used in the first four stages in the division chain (divide-by-8 circuit and the first stage of divide-by-16 circuit), due to their speed under low power-supply conditions. The low-frequency division (last three stages of the divide-by-16 circuit) is implemented with static master–slave type DFFs.

The operation of the modulator is as follows. The modulator clock generated by the divide-by-128 circuit increments a 3-bit counter, the output of which is decoded to select the transmit bit in a round-robin fashion from the 8-bit data word. A 7-Mb/s data rate is achieved. The differential output of the LC oscillator is connected to the PA through a two-input two-output multiplexer. The value of the selected transmit bit determines how the multiplexer routes the oscillator's differential output to the differential input of the power amplifier. In this way, when the transmit bit changes from 0 to 1 or from 1 to 0, the phase of the modulated output changes by 180 degrees. A nonoverlap circuit generates the gate signals to the four NMOS switches of the multiplexer, ensuring break-before-make switching, preventing the oscillator outputs from being inadvertently shorted together.

F. Power Amplifier

A class-B push-pull stage is used to drive a 50-Ω antenna. It delivers a total balanced output power of -24 dBm to the 50-Ω load. One of the two identical halves of the pseudo-differential class-B power amplifier is shown in Fig. 12.

Transistors M3, M4, and M5 set up the quiescent gate voltages for the NMOS and PMOS output devices (M1 and M2). The W/L ratios of bias transistors are adjusted so that gate–source voltages of M1 and M2 are biased just below the threshold voltage, $V_{\rm TH}$, to achieve class-B operation. The RF input signal $(V_{\rm RF\_IN})$ comes directly from the BPSK modulator, while the bias generator supplies the gate voltage for M4 $(V_{\rm BIAS})$. Capacitors C1 and C2 couple $V_{\rm RF\_IN}$ to the gates

TABLE I
SUMMARY OF THE MEASURED RESULTS OF THE 900-MHz TELEMETRY DEVICE

Carrier Power	-24 dBm on 50Ω	
Max Oper. Range of RF-DC	18.3 meters (7 W base station power)	
Data Rate	7 Mbits/sec	
Power Consumption	**Standby**	**Active**
	<900 nA	2 mA
Phase Noise @ 10kHz offset	**Free Running**	**Locked @ f/2**
	-88.5 dBc/Hz	-99.1 dBc/Hz
FOM	167 dBc/Hz	178 dBc/Hz

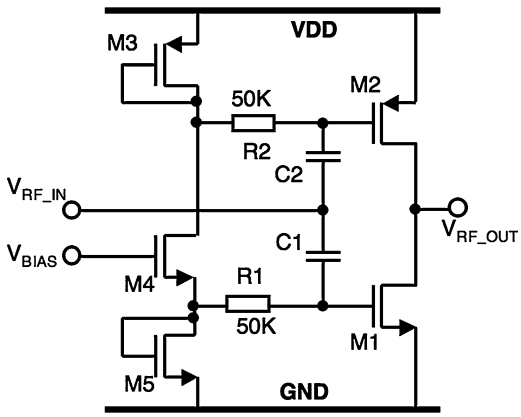

Fig. 12. Schematic of the class-B power amplifier.

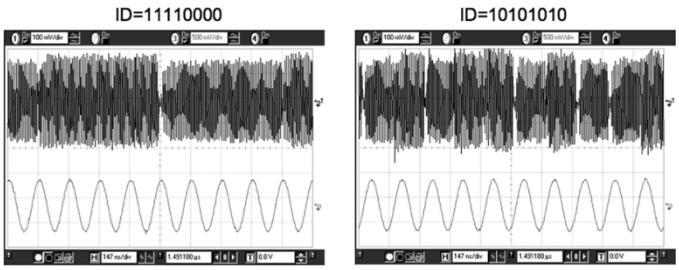

Fig. 13. Captured transmit signals for two ID words along with a reference clock.

of the output transistors M1 and M2. Resistors R1 and R2 block injection of the RF input into the bias branch, increasing efficiency.

Transmitted modulated 900-MHz signals from the prototype device were captured and verified with the help of an 8-GSample/s oscilloscope and a spectrum analyzer. Captured transmit signals for two different words, along with a bit-rate reference clock, are shown in Fig. 13. The output spectrum of the BPSK modulated 900-MHz signal is shown in Fig. 14.

III. SUMMARY

The device was fabricated in 0.25-μm mixed-mode TSMC CMOS with a thick-top-metal option. A die microphotograph is given in Fig. 15. The IC packaged in a 52-pin ceramic LCC package is surface mounted on an impedance-matched PCB. The active area of the telemetry device is less than 1 mm^2. The system is fully integrated with the exception of an off-chip storage capacitor. The prototype incorporates ESD protection on all pins. A summary of the test results is given in Table I.

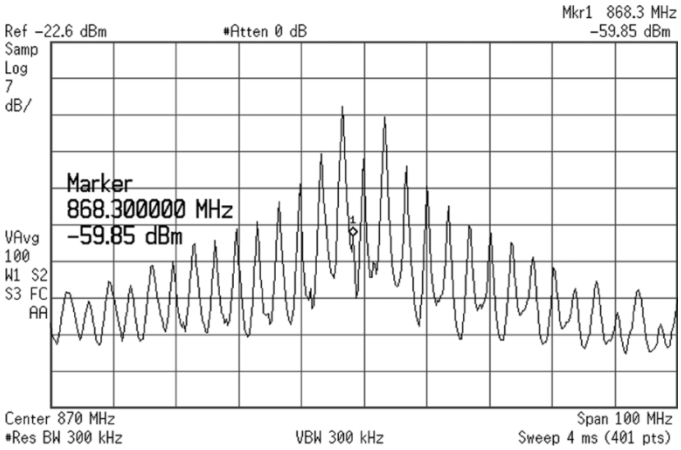

Fig. 14. Output spectrum for ID=10101010.

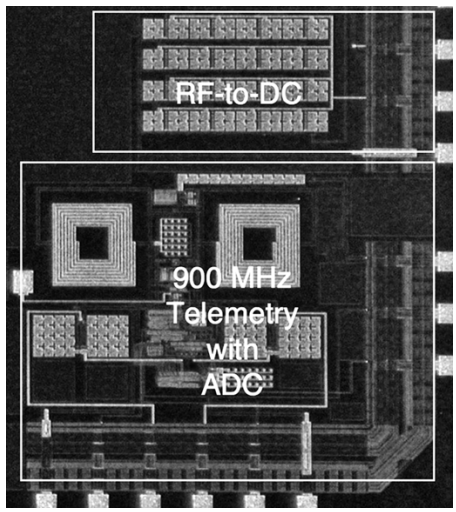

Fig. 15. Die microphotograph.

IV. CONCLUSION

We present a new architecture for efficient power transfer that increases the operational range of a batteryless wireless transponder. A new, low-power clock extraction technique based on injection-locking is used to generate a low-phase-noise system clock. This generates a very low-phase-noise 900-MHz clock, locked onto a superharmonic or subharmonic of the incident RF signal. Binary phase-shift keying is employed for data transmission.

The circuit is fabricated in TSMC 0.25-μm mixed-mode process with thick-top-metal option. A wireless operation range

of the RF–DC converter of more than 18 meters is indicated by anechoic chamber testing.

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REFERENCES

[1] S. Masui, E. Ishii, T. Iwawaki, Y. Sugawara, and K. Sawada, "13.56 MHz CMOS RF identification transponder integrated circuit with a dedicated CPU," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1999, pp. 162–163.

[2] Q. Huang and M. Oberle, "0.5-mW passive telemetry IC for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 937–946, Jul. 1998.

[3] M. Ghovanloo and K. Najafi, "A high-rate frequency shift keying demodulator chip for wireless biomedical implants," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2003, vol. 5, pp. 45–48.

[4] E. H. J. Callaway, *Wireless Sensor Networks: Architectures and Protocols:*. New York: Auerbach, 2004.

[5] A. DeHennis and K. D. Wise, "A double-sided single-chip wireless pressure sensor," in *Proc. IEEE Int. Conf. Micro Electro Mechanical Systems (MEMS)*, Jan. 2002, pp. 252–255.

[6] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7 μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[7] F. Kocer, P. M. Walsh, and M. P. Flynn, "An injection locked, RF powered, telemetry IC in 0.25 μm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2004, pp. 24–27.

[8] M. Ghovanloo and K. Najafi, "A high-rate frequency shift keying demodulator chip for wireless biomedical implants," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2003, vol. 5, pp. 45–48.

[9] J. D. Cockcroft and E. T. S. Walton, "Experiments with high velocity positive ions. (I) Further developments in the method of obtaining high velocity positive ions," in *Proc. Royal Soc. London, Series A*, Jun. 1932, vol. 136, pp. 619–630.

[10] D. K. Cheng, *Field and Wave Electromagnetics*. Reading, MA: Addison Wesley, 1989.

[11] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. Oxford, U.K.: Oxford Univ. Press, 2002.

[12] F. Kocer, P. M. Walsh, and M. P. Flynn, "Wireless, remotely powered telemetry in 0.25 μm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2004, pp. 339–342.

[13] C. R. Poole, "Subharmonic injection locking phenomena in synchronous oscillators," *Electron. Lett.*, vol. 26, pp. 1748–1750, Oct. 1990.

[14] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.

[15] C. R. Neagu, H. V. Jansen, A. Smith, J. G. E. Gardeniers, and M. C. Elwenspoek, "Characterization of a planar microcoil for implantable microsystems," *Sensors Actuators, A: Phys.*, vol. 62, pp. 599–611, Jul. 1997.

[16] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1018–1024, Jul. 2001.

[17] Y. A. Eken, "High frequency voltage controlled ring oscillators in standard CMOS," Ph.D. dissertation, Dept. Electr. Comput. Eng., Georgia Inst. Technol., Atlanta, GA, 2004.

[18] M. Afghahi, "A robust single phase clocking for low power, high-speed VLSI applications," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 247–254, Feb. 1996.

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