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A 3.6mW 2.4-GHz Multi-Channel Super-Regenerative Receiver in 130nm CMOS

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Abstract–**Super-regeneration is re-examined for its simplicity and power efficiency for low-power, short-range communication. Although previous approaches rely on a high quality off-chip LC-tuned circuit, this paper describes a fully integrated 2.4-GHz ISM band super-regenerative receiver implemented in 130 nm CMOS. Several new design features, that take advantage of digital processing, are proposed. A synthesizer scheme tunes the circuit for multi-channel operation. Frequency selectivity is improved through Q-enhancement. The entire receiver occupies less than 1 mm^2, and consumes 3 mA from a 1.2 V supply, with a data rate of up to 500 Kbps, an energy per received bit of 7.2 nJ/bit, a channel spacing of 10 MHz, and a sensitivity of –80 dBm.**

I. Introduction

Applications such as sensor networks, implantable neuroprosthetic devices, robotics, and home automation, require low data rate, short-range wireless communication. For these applications, power consumption must be very low and size must be small. A candidate architecture is *super-regeneration*, a technique originally proposed by Armstrong in 1922 [1]. The extraordinary gain and simplicity of the super-regenerative scheme promise low power consumption and small circuit area [2]. However, the poor frequency selectivity of traditional super-regenerative receivers limits use in practice. Previous integrated implementations of super-regeneration require very fine analog control of biasing to optimize performance, and also require a high quality off-chip LC-tuned circuit [2]. Furthermore, these designs are also limited to single-channel operation.

We re-examine super-regeneration and demonstrate a new fully integrated, multi-channel wireless receiver architecture. The architecture incorporates a Q-enhanced filter, greatly improving frequency selectivity. Instead of using an analog quench signal, quenching of the super-regenerative oscillator is achieved with a current digital-to-analog converter (DAC) to gain better control. A phase-locked loop scheme tunes the frequency of a super-regenerative oscillator, making robust multi-channel operation feasible. Whereas other designs rely on an off-chip tuned circuit, the prototype IC, fabricated in 130 nm CMOS is completely integrated. The receiver has a power consumption of 3.6 mW and a data rate of 500 Kbps, resulting in an energy per received bit of 7.2 nJ/bit. It also occupies less that 1 mm^2, and has a sensitivity of –80 dBm.

II. Super-regeneration and Q-Enhancement

The super-regenerative technique is based on the startup of a harmonic oscillator [3]. The *startup time* is defined as the time required for the oscillation to reach saturation after the oscillator is turned on. The oscillation builds up from fluctuation across the oscillatory nodes. When an external signal is injected onto the oscillatory nodes, oscillation builds up more quickly. Thus, signal detection is achieved by observing the difference in startup time caused by the presence of a signal – this scheme is well suited for the detection of on-off keying modulation.

Fig. 1 shows a parallel-tuned circuit which forms the core of the oscillator. The input signal is represented by an equivalent current source of amplitude A and radian frequency ω. G_0 is a shunt conductance representing the parasitic loss of the tuned circuit and $-G_a$ represents the negative conductance provided by active devices. In an oscillator, active devices compensate for loss in the resonant tank and the overall conductance $G = G_0 - G_a$ can be either positive or negative.

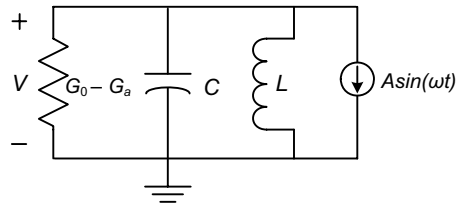

Fig. 1. Parallel-tuned circuit representing a harmonic oscillator.

The voltage V across the circuit can be expressed as

$$C\frac{dV}{dt} + GV + \frac{1}{L}\int V dt = A\sin(\omega t)\cdot \tag{1}$$

The complete solution of the equation can be written as

$$V = k_1 e^{(-\alpha + j\omega_d)t} + k_2 e^{(-\alpha - j\omega_d)t} + \frac{A\sin(\omega t + \phi)}{\sqrt{G^2 + (\omega C - 1/\omega L)^2}} \tag{2}$$

where

$$\alpha = G/2C \quad \text{and} \quad \omega_d = \sqrt{\frac{1}{LC} - \left(\frac{G}{2C}\right)^2} = \sqrt{(\omega_0^2 - \alpha^2)}.$$

The first two terms of (2) represent a transient oscillation at frequency ω_d with a damping factor, α, which is directly proportional to G. If G is positive, the tuned circuit loses energy and the oscillation decays. However, if G is negative, the active devices add energy to the resonant circuit, building up an oscillation from the initial voltage, which is represented by coefficients k_1 and k_2. This special case is termed *super-regeneration*. A large absolute value of G results in a more rapid growth in oscillation and higher super-regenerative gain. Equation (2) also suggests that the oscillation grows to infinity, but in reality the amplitude is limited by the nonlinearity of the active components.

Since super-regeneration amplifies *any* initial voltage, super-regeneration provides little frequency selectivity, limiting its usefulness in practical communication applications. Frequency selectivity needs to be improved to suppress out-of-band signals. This filtering is done with the help of the LC-tuned circuit at the core of the oscillator. The last term of (2) indicates a band-pass response centered at frequency $\omega_0 = 1/\sqrt{LC}$, and the quality factor Q of the tuned circuit can be expressed as

$$Q = \frac{1}{G_0 - G_a}\frac{1}{\sqrt{L/C}}. \quad (3)$$

We note that Q becomes larger, improving filtering, as G_a approaches G_0. This technique is known as Q-enhancement [4]. For better signal selectivity, the tuned circuit is first operated in Q-enhanced mode to suppress out-of-band signals and then in super-regenerative mode to amplify the desired in-band signal. For a cross-coupled LC oscillator, since $G_a = g_m/2$ and g_m is related to drain current, the circuit is switched between the Q-enhanced and super-regenerative modes simply by changing the bias current of the LC oscillator.

III. Receiver Description

We now describe the overall architecture and operation of the super-regenerative receiver.

A. System Architecture

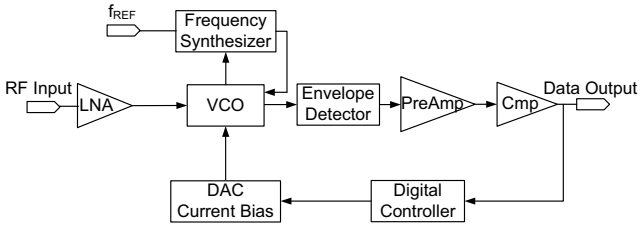

Fig. 2. Proposed architecture of the super-regenerative receiver.

The prototype (Fig. 2) incorporates a low noise amplifier (LNA), a voltage-controlled oscillator (VCO), an envelope detector, a pre-amplifier, a comparator, a frequency synthesizer, a DAC current source, and a digital controller. The RF input is first amplified by the LNA and then fed to the VCO. The VCO serves as a narrow-band filter, or a super-regenerative oscillator, depending on the amount of bias current. The envelope detector detects the amplitude of the oscillation. The detector's output is amplified by a preamplifier and sampled by a comparator. The comparator output supplies digital demodulated data. The architecture employs novel digital control of quenching. To achieve this, the digital controller sets the current DAC to control the bias current of the VCO. A frequency synthesizer tunes the resonant tank so that the tuned circuit has the correct center frequency. The feedback divider of the PLL is programmable, allowing the receiver to be tuned to different channels.

B. Critical Current and Quench Mechanism

From (3), if G_a equals G_0, Q tends towards infinity. The critical current I_{crit} is the value of bias current that results in G_a being equal to G_0. If the bias current is larger than I_{crit}, then G_a is greater than G_0, and the circuit is in super-regenerative mode. Otherwise, the circuit operates as a Q-enhanced filter. The bias current is controlled by a quench signal, periodically switching between these two modes. Traditionally, this quench signal is an analog signal and the shape of the quench signal must be carefully considered to achieve good performance [2]. In this work, we use a current digital-to-analog converter to generate the bias current for the oscillator. A digital controller generates the corresponding digital value of the quench signal. The minimum DAC value that results in oscillation is used as I_{crit}. Once I_{crit} is known, the quality factor of the tuned circuit is maximized, giving the filter a narrow passband, by setting the current DAC just one LSB below I_{crit}.

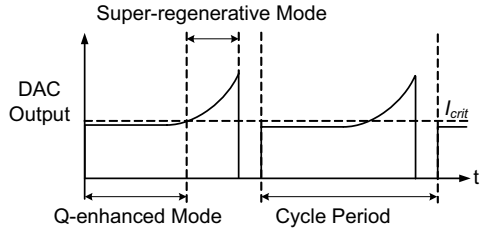

Fig. 3. Output waveform of the current DAC.

Fig. 3 shows the output waveform of the current DAC, in normal operation. During each period, the bias current is first set just below I_{crit} so that the circuit operates in Q-enhanced mode, suppressing out-of-band signals. Next, the bias current is increased slowly at the beginning and then more rapidly with time, to achieve both a smooth transition to the super-regenerative mode and a sufficient gain to detect the input signal. This current waveform can be easily created with the help of the current DAC. At the end of the cycle, the bias current is turned off to disable any oscillation.

IV. Building Blocks

We now discuss the major components of the receiver.

A. Low Noise Amplifier and Voltage-Controlled Oscillator

A fully-differential common-source LNA is used in this design [5]. The RF inputs are AC-coupled to the LNA and the input impedance is matched to 50 Ω for maximal power delivery. As shown in Fig. 4, the VCO is a differential cross-coupled LC oscillator. The inductors are implemented with on-chip spiral coils, and two hyper-abrupt junction varactors are used to tune frequency. The cross-coupled transistors, M1 and M2, provide negative conductance, controlled by the current DAC, compensating for loss in the LC-tuned circuit. The outputs of the VCO are connected to the envelope

detector and to the frequency synthesizer. These nodes also serve as the inputs for signals coming from the LNA.

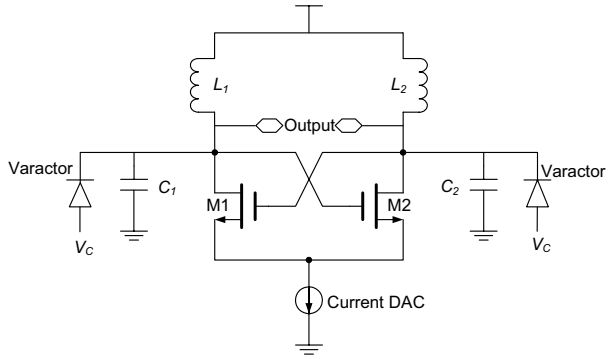

Fig. 4. Schematic of the voltage-controlled oscillator.

B. Envelope Detector

A schematic of the envelope detector is shown in Fig. 5. V_{inp} and V_{inn} are connected to outputs of the VCO. V_{outp} rises with the growth of VCO oscillation. Note that transistors M3–M6 are small to ensure operation at 2.4 GHz.

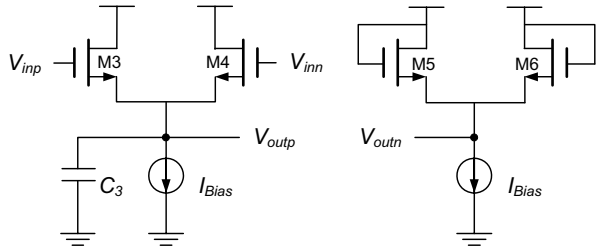

Fig. 5. Schematic of the envelope detector.

C. Pre-Amplifier and Comparator

Fig. 6 shows a simplified diagram of the pre-amplifier and comparator. Offset cancellation at the output of the pre-amplifier eliminates the offset of the preceding stages. Switches S_1 and S_2 are closed when the oscillator is turned off to store the offset on capacitors C_4 and C_5, and then opened during the comparison operation. The comparator consists of two differential input stages, two regenerative flip-flops, and an SR latch [6]. The comparator is configured so that data output equals logic zero when no oscillation occurs (V_{inp} equals V_{inn}). Once V_{inp} rises, indicating oscillation, the data output becomes logic one.

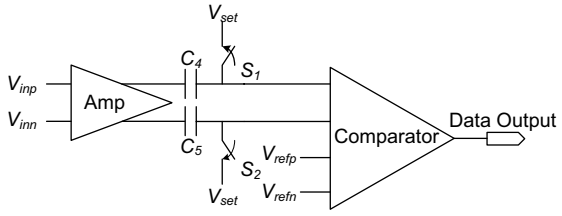

Fig. 6. Simplified diagram of the pre-amplifier and comparator.

D. Current DAC

Since the precision of the bias control directly affects the system performance, a 9-bit current DAC with an LSB size of 2 μA is used. Monotonicity is important to ensure the smooth growth of output current required for signal detection. A segmented architecture is adopted to guarantee monotonicity yet minimize complexity. The 3 MSBs are thermometer-coded and the 6 LSBs are binary-coded.

E. Frequency Synthesizer

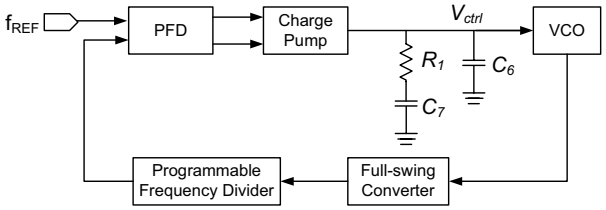

Fig. 7. Block diagram of the frequency synthesizer.

Fig. 7 shows a block diagram of an integer-N frequency synthesizer. A type-II PLL is used and the loop dynamics are determined by the second-order loop filter. A full-swing converter amplifies the VCO outputs to CMOS levels to be processed by the digital frequency divider. The divider is programmable from 480 to 496 in steps of 2. With a frequency reference of 5 MHz, the frequency synthesizer can generate 9 different frequencies corresponding to the 9 receiver channels, spaced 10 MHz apart, from 2.4 GHz to 2.48 GHz.

F. Digital Controller

The digital circuitry of the receiver runs under a 5-MHz system clock. It controls the current DAC when switching between frequency tuning and detection (filtering and super-regeneration). The system first runs the frequency synthesizer to tune the frequency to the desired channel. Next, the system enters detection mode. In this mode, the DAC current source generates the bias current waveform illustrated in Fig. 3. Each detection period spans ten clock cycles. During the first four cycles, the receiver operates in Q-enhanced filter mode. During the next five cycles, the receiver operates in super-regenerative mode. Finally, the oscillator's bias current is turned off during the last cycle, quenching any oscillation. The comparator is enabled during the last six cycles. The comparator output becomes logic one, if and when the VCO oscillates, and is reset to logic zero during the last cycle. In this way, the startup time of the oscillation is reflected by the number of 1's in the data output per detection period. The maximum data rate is 500 Kbps.

V. MEASUREMENTS

The prototype is implemented in 130 nm mixed-mode CMOS. Fig. 8 shows a photomicrograph of the IC. The device has an area of 1 mm^2, is packaged in a 68-pin LCC package and surface mounted on a test PCB. Due to parasitics, the frequency range of the synthesizer is 2.28–2.36 GHz.

We focused our evaluation on the 2.31-GHz channel. First we measured the average number of 1's in the data output per period with respect to input power of a signal from desired

channel. Fig. 9 shows that the receiver has a sensitivity of –80 dBm. Next, we applied a signal in an adjacent channel, 10 MHz from the desired frequency. Fig. 9 shows this signal is rejected by the receiver, confirming the excellent frequency selectivity of this architecture.

We measured the bit error rate by applying a –70-dBm on-off keying modulated input and no error was detected in 1000 symbols. The receiver consumes 3 mA from a 1.2 V supply. The measured performance of the system is summarized in Table I.

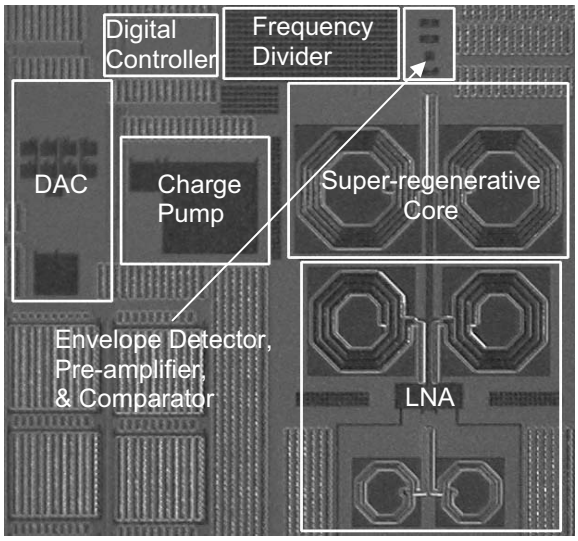

Fig. 8. Photomicrograph of the receiver.

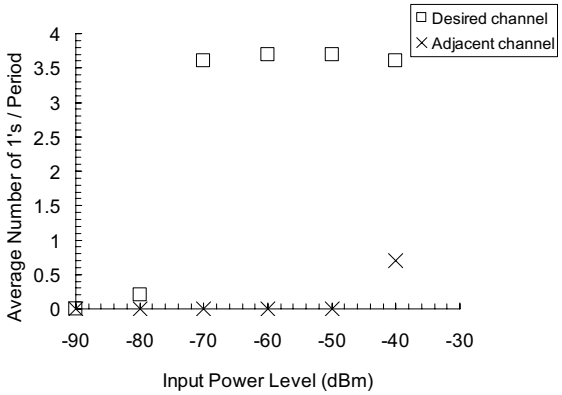

Fig. 9. Average number of 1's in the data output per period versus power level of desired and adjacent channel input signals.

VI. Conclusion

We present a fully integrated super-regenerative receiver in 130 nm CMOS. A new architecture incorporates a current DAC allowing sophisticated control of the super-regenerative circuit and Q-enhanced filtering. The use of an on-chip LC-tuned circuit, with a frequency synthesizer, enables multi-channel communication and reduces the overall size to 1 mm^2. As shown in Table II, our receiver has the lowest value of energy per received bit, and it is believed to be the only fully integrated super-regenerative receiver with multi-channel capability.

Acknowledgment

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TABLE I

Summary of Measurements

Operating voltage	1.2 V
Supply current	3 mA
Operating frequency	2.28 GHz to 2.36 GHz
Quench frequency	500 kHz
Sensitivity	–80 dBm
Data rate	< 500 Kbps
Channel spacing	10 MHz
Bit error rate (–70 dBm input)	< 1/1000

TABLE II

Comparison of Receiver Performance

	[2]	[7]	[8]	This work
Receiver architecture	Super-regeneration	Low-IF	Direct RF-sampling	Super-regeneration
Standard	—	802.15.4	Bluetooth	—
Power	1.2 mW	21 mW	58 mW	3.6 mW
Data rate	100 Kbps	200 Kbps	1 Mbps	500 Kbps
Energy per bit	12 nJ/bit	105 nJ/bit	58 nJ/bit	7.2 nJ/bit
Operating frequency	1 GHz Single-channel	2.4 GHz Multi-channel	2.4 GHz Multi-channel	2.4 GHz Multi-channel
Technology	0.35 CMOS	0.18 CMOS	0.13 CMOS	0.13 CMOS