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An Injection Locked, RF Powered, Telemetry IC in 0.25μm CMOS

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Abstract

This wireless transponder recovers power and a reference clock from an incident RF signal and returns data on a 900MHz carrier. A multi-stage voltage multiplier/rectifier converts the received low power RF signal to a useful DC voltage and stores the energy on a storage capacitor. The injection locking technique facilitates power efficient generation of a low phase noise 900MHz internal clock from the received 450MHz signal by employing a fully integrated low power LC oscillator. A fully integrated pseudo-differential power amplifier operating in class AB regime is used as the output stage of the system. The system dissipates an average of 5μA in standby mode and 1.1mA during active operation.

Introduction

Wireless, batteryless, systems and sensors have applications in biomedical systems [1], smart card readers, RFID [2], and environmental monitoring [3]. Wireless transmission of power eliminates the battery, making the system far smaller, more reliable and of lower cost by avoiding regular battery maintenance.

A block diagram of a conventional active telemetry system is given in Fig. 1. Both the system clock and system power are extracted from the incident RF signal. An RF to DC converter rectifies the incident RF radiation and stores the energy on a storage capacitor. The system clock is modulated and fed to the power amplifier to be transmitted.

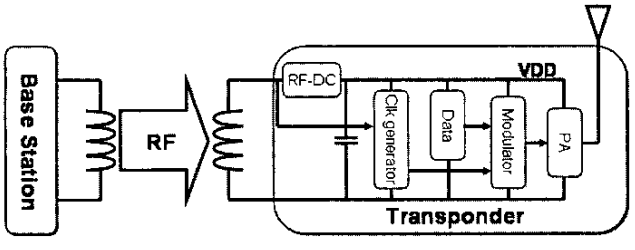

Fig. 1. The block diagram of conventional active telemetry

In a conventional system, a full-wave or a half-wave rectifier usually performs the RF to DC conversion. However, with this approach the amplitude of the received signal must be large enough to overcome the junction voltage of the diodes in the rectifier. Since the maximum power transmitted from a base station cannot exceed FCC regulations, the separation between the base station and the transponder is limited (often in millimeters [4]).

In most implementations, a Schmitt trigger circuit recovers a system clock from the incident signal. Frequency multiplication and division methods, such as the use of a PLL, separate the output carrier frequency from the incident RF frequency. These circuits are complex and consume additional power. In practice, the power consumption of the Schmitt trigger limits the maximum frequency to 10s of MHz. Furthermore, Schmitt trigger based clock recovery is prone to phase noise and jitter, especially for low amplitude incident signals, limiting range.

We propose a new RF-DC conversion method, which generates a useful DC voltage even with very small incident signal amplitude. It is composed of a series of clockless voltage multipliers and can operate under very low input signal levels. Furthermore, we propose a new clock recovery technique, based on an injection locked LC oscillator. Very low power, low phase noise and phase jitter clock recovery is achieved even with very small input signal amplitudes.

System Overview

A block diagram of the proposed system is given in Fig. 2. A high efficiency RF-DC converter generates a DC voltage much higher than the peak amplitude of the incident RF signal and stores the energy on a large storage capacitor. This generated DC voltage is used as the supply of the system.

Unlike more conventional RF powered systems, this telemetry IC accumulates energy in standby mode, increasing the range from base and reducing base transmit power.

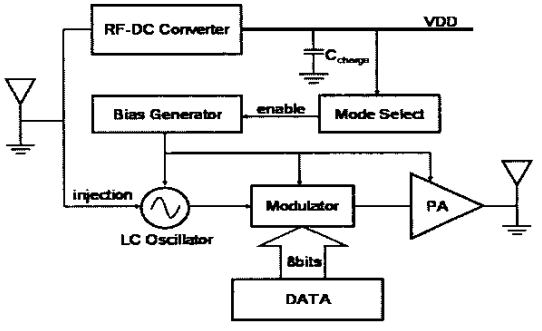

Fig.2. The block diagram of the proposed architecture

A mode select circuit detects when the capacitor voltage exceeds a threshold (2.5V), powering up the telemetry circuitry. The system continues to operate until the capacitor voltage drops below a lower threshold (1.5V). At this point,

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the telemetry circuit is powered down, allowing the capacitor to recharge. Given a sufficiently high received power level the telemetry circuit can operate continuously.

A key feature of this approach (unlike other designs [5]) is that there is no on-chip supply regulation. This saves power and chip area. Simple regulators such as source followers are inefficient and rely on a relatively accurate reference voltage from a zener or bandgap reference. Instead, by tolerating large swings in supply voltage we can efficiently discharge and utilize the power stored on the capacitor. On the other hand, all system blocks must now operate over a large supply range (2.5V to 1.2V) with low supply sensitivity.

For a given capacitor size and receive power, the duration of active operation and the duty cycle of the system are determined by the total power consumption. Therefore, all circuitry is designed for minimum power dissipation.

An on-chip LC oscillator generates the system clock. The LC oscillator is injection locked to an integer multiple (or fraction) of the incident RF signal. A continuous wave modulator and a power amplifier (PA) working in class AB regime modulate the transmit data on a 900MHz carrier.

A. RF-DC Converter

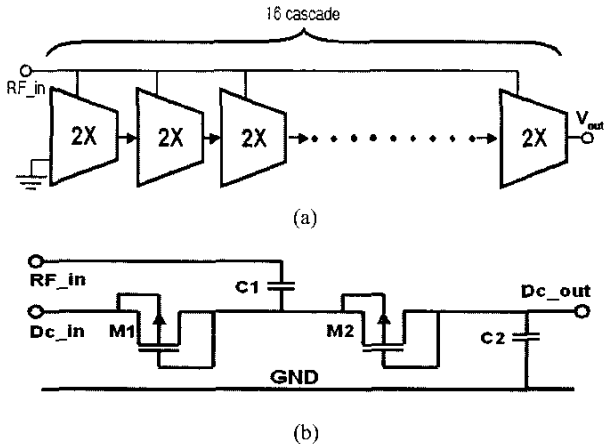

Fig.3. (a) Block diagram, (b) schematic of the voltage multiplier

A Dickson [6] multiplier circuit with multiple stages generates a DC voltage higher than the peak signal amplitude at the receiving port. A block diagram and the schematic details of a stage are given in Fig. 3. The Dickson voltage multiplier does not incorporate active switches eliminating switching losses. Diodes are implemented as diode-connected low V_T PMOS transistors to achieve low voltage operation. The minimum voltage swing required for operation is only 100mVpeak. With a $150mV_{pcak}$ input signal, a conversion efficiency of more than 80% is achieved. A cascade of 16 stages is used to generate and store 2.5V on the storage capacitor to power the system.

B. System Clock Generation

A reference clock is extracted from the incident RF signal using an injection locked LC oscillator [8]. Injection locking is far more power efficient than a Schmitt trigger scheme and delivers a recovered clock with very low phase noise and phase jitter. The low power LC oscillator, shown in Fig. 4, lies at the heart of the injection locking scheme. For low voltage operation, the oscillator uses only NMOS cross-coupled devices (M7, M8). The oscillator is operated in current limited mode [7] to minimize dissipated power. For low power consumption, we achieve maximum effective tank resistance, by maximizing inductance.

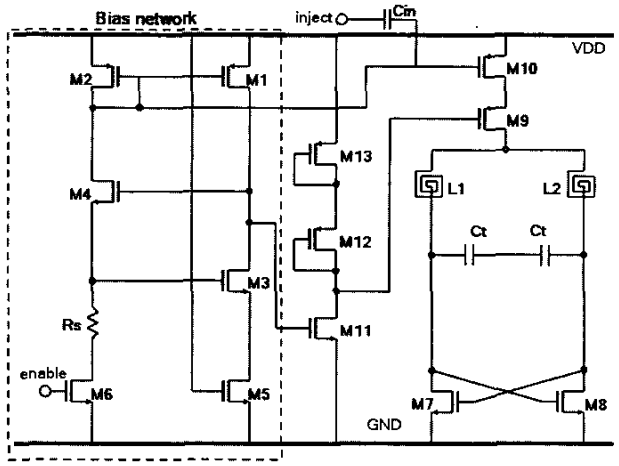

Fig.4. LC oscillator and the bias network

The received RF carrier is capacitively coupled to the tail of the oscillator to achieve injection locking. The oscillator can lock to a signal with a frequency close to the 900MHz free running frequency or an integer fraction or multiple of this frequency. Injection locking makes it possible to efficiently generate a clock signal that is an integer multiple (or integer fraction) of the RF power signal frequency without the complexity, area and power consumption of a PLL. This allows the received and transmitted signal frequencies to be separated without additional power dissipation.

The bias circuit is designed for minimum oscillator supply sensitivity while dissipating only 12μA. In this bootstrapped bias string (Fig. 4), the voltage drop across resistor Rs equals the gate-source voltage of transistor M3, setting the bias current. Transistor switch M6 enables the oscillator bias. The enable signal is generated by the mode-selector, discussed in the next subsection. M5 compensates for the voltage drop across the switch, M6. For a free running oscillator (no injection lock) the measured oscillation frequency varies by 70KHz over a supply voltage variation from 1.5V to 2.5V, giving an oscillation frequency supply sensitivity of only 70ppm/V.

C. Mode Selector

The mode selector circuit (Fig. 5) decides whether the system operates in the standby mode (i.e. charging) or operates normally. In the standby mode, the system waits for the capacitor to charge and dissipates very little current. The time required to charge the capacitor depends on the power received and the power dissipated. During this phase, it is essential that the current dissipation is low. In the standby mode, the system dissipates only 5μA.

The system is enabled by the mode-selector circuit when the voltage stored on the storage capacitor exceeds 2.5V. When enabled, the system draws current from the capacitor, discharging it. The system is put back in standby mode, dissipating very little current when the voltage on the storage capacitor drops below 1.5V.

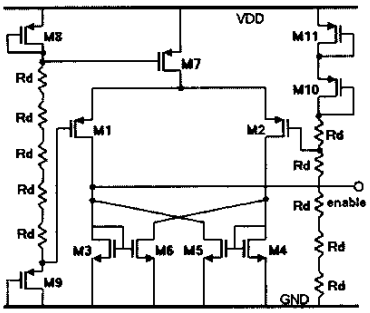

Fig.5. Schematic of the mode selector

D. Modulation

A continuous wave (CW) modulation technique is employed for its simplicity and low power consumption. Continuous wave modulation is an extreme case of amplitude modulation, where the carrier is completely turned off to transmit a "ZERO." This on-off keying technique is achieved by enabling and disabling the power amplifier (Fig. 6). Disabling the power amplifier during the "off" period reduces the power consumption of the power amplifier by 50%.

A divide-by-16 circuit is constructed with true single phase D-flip-flops (TSP-DFF). Medium threshold transistors deliver fast operation under low supply voltages. The divider output is fed to a 3-bit counter, then to a 3-to-8 decoder to serialize the 8-bit data word. Depending on each bit value, the input to the power amplifier is either connected to the output of the oscillator or connected to the ground.

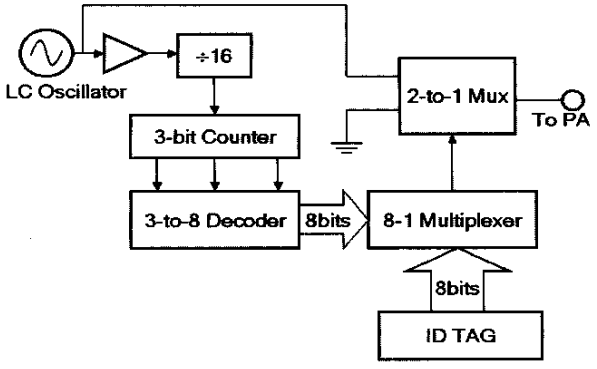

Fig.6. Block diagram of the CW modulator

Test Results

In order to test the functionality of the mode-selector circuit, the voltage on the charging capacitor is swept between 0V and 2.6V and the current dissipated by the system is plotted (Fig. 7). The hysteresis curve with thresholds at 1.5V and 2.5V clearly indicates the mode of the operation.

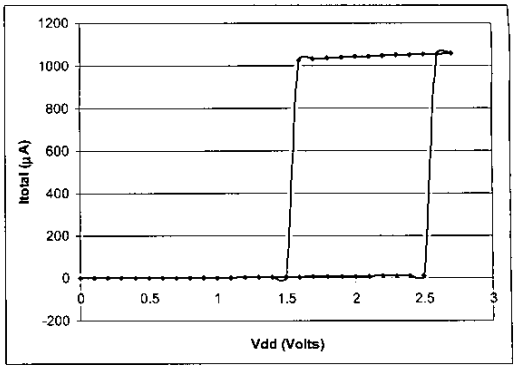

Fig.7. Test results of the mode selector

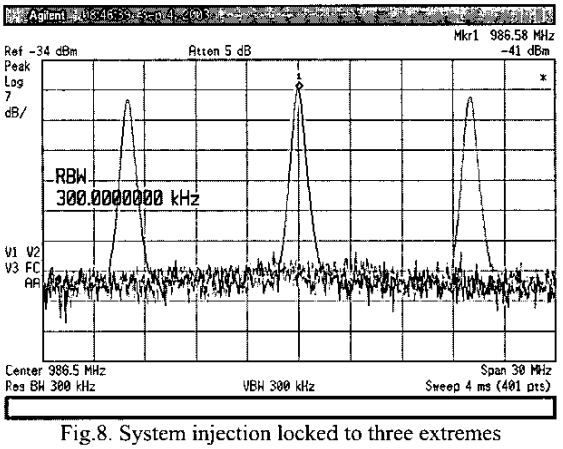

Fig.8. System injection locked to three extremes

The proposed clock recovery technique is tested by locking onto a sub-harmonic frequency (450MHz) of the free running oscillator. A locking range of 20MHz is achieved with 150mV input signal amplitude. Fig. 8 shows the output of the system locked onto three extreme cases.

The measured phase noise of a free running oscillator (no injection lock) is -94dBc/Hz at an offset of 100KHz. This drops to -103dBc/Hz when the oscillator is locked to f/2 harmonic as shown in Fig.9.

The figure of merit (FOM) [9] of the free running system is calculated as 175dBc/Hz. This improves to 185dBc/Hz when locked to f/2 subharmonic and to 192dBc/Hz when locked to 2f superharmonic.

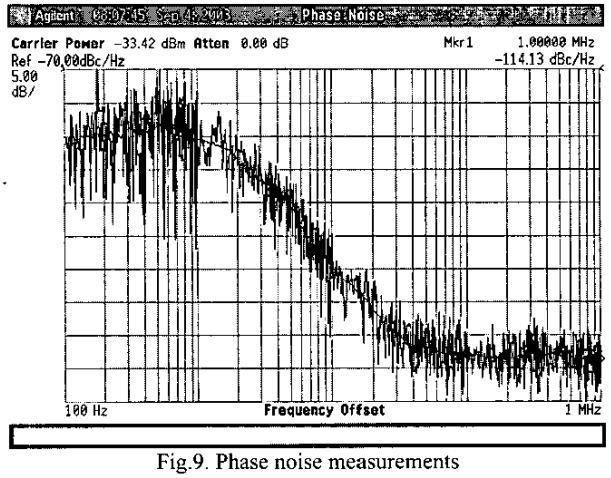

Fig.9. Phase noise measurements

The transmitted modulated 900MHz signal from the device was captured and verified with the aid of a direct conversion receiver. In this test, the device was injection locked to a 450MHz clock, while the power amplifier output was mixed with a 900MHz clock and low pass filtered. The demodulated waveforms for four different ID values are shown in Fig. 10.

The design was fabricated in 5 metal TSMC 0.25μm CMOS with low V_T transistors and thick top metal. The active area of the design (excluding storage capacitor) is $1mm^2$. The IC was packaged in a 52 pin ceramic LCC package. The prototype incorporates ESD protection. A die microphotograph is given in Fig. 11.

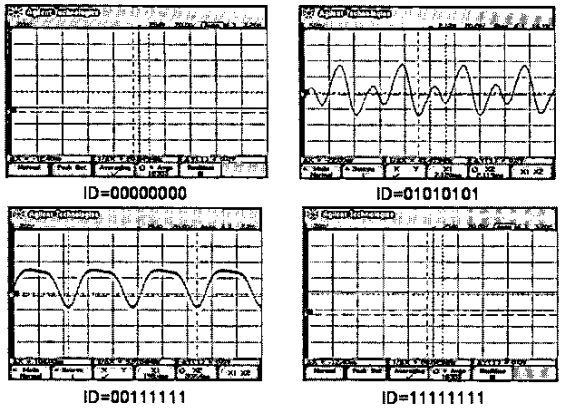

Fig.10. Demodulated output for four ID inputs

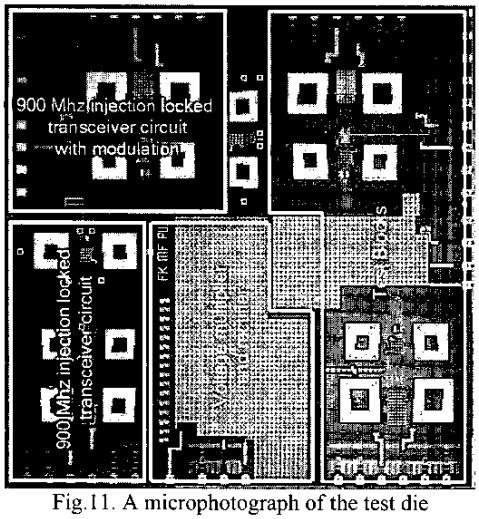

Fig.11. A microphotograph of the test die

Conclusion

We present a new architecture for efficient power transfer increasing the operational range of a batteryless wireless transponder. A new, very low-power clock extraction technique based on injection locking is used to generate a low phase noise system clock. This generates a very low phase noise 900MHz clock locking onto a super-harmonic or sub-harmonic incident RF signal. A continuous wave (CW) modulation technique is employed for data transmission for its simplicity and low power consumption. The circuit is fabricated in TSMC 0.25μm mixed-mode process with thick-top-metal option. A summary of the system is given in Table 1.

Table 1. Summary of the system

Technology	TSMC 0.25μm with thick top metal		
Active area	~1mm^2		
Modulation	Continuous Wave		
Carrier Frequency	900Mhz		
Power Consumption		**Standby**	**Active**
	Oscillator	0	450μA
	PA	0	650μA
	Free Running	**Locked @ 450 Mhz**	**Locked @ 1.8 Ghz**
Ph. Noise (dBc/Hz)	-94	-103	-112
FOM (dBc/Hz)	175	181	194

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