Digital Calibration Incorporating Redundancy of Flash ADCs

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***Abstract*—As feature size and supply voltage shrink, digital calibration incorporating redundancy of flash analog-to-digital converters is becoming attractive. This new scheme allows accuracy to be achieved through the use of redundancy and reassignment, effectively decoupling analog performance from component matching. Very large comparator offsets (several LSBs) are tolerated, allowing the comparators to be small, fast and power efficient. In this paper, we analyze this scheme and compare with it with more traditional approaches.**

***Index Terms*—Analog-to-digital conversion , analog redundancy, calibration, flash.**

I. Introduction

FAST low-resolution CMOS analog-to-digital converters (ADCs) required in applications such as hard-disk-drive read channel, Gigabit Ethernet, and wireless receivers, are most often implemented with the Flash technique. At 5–7 bits of resolution, Flash ADCs achieve higher sampling speeds, and because of their analog simplicity are more suited to deep-submicron processes than other types of ADCs.

In Flash ADCs, comparator offset must be controlled to avoid nonmonotonicity or large errors. In CMOS, this is traditionally accomplished through device sizing [1], offset nulling [1], [2], [3], averaging [4], [5], and digitally controlled trimming [6]. The first of these techniques relies on the improvement in transistor matching that is associated with increased transistor size. Offset nulling techniques, often implemented with the help of switched-capacitor offset-cancelled preamplifiers, are more power efficient [1]; however, these techniques may not allow continuous conversion and SC circuits are difficult to implement in low-voltage processes. Preamplifier output offset can be reduced through spatial filtering [4]. Interpolation can reduce the ADC differential nonlinearity (DNL) due to pre-amplifier offset [7]. In another technique, digitally controlled currents cancel comparator offset [6].

We propose digital calibration based on comparator redundancy and simple digital processing to cancel offset. This technique allows good performance to be achieved in the presence of large comparator offsets, without preamplifiers or analog-offset cancellation. Earlier in [8], [9], we presented a 6 bit prototype ADC along with experimental results. In Section II, we review the basics of the new technique. Section III explains the benefits of this scheme, while a more detailed analysis is presented in Section IV. Section V discusses design tradeoffs, including edge-effects, the amount of redundancy, and the accuracy and resolution required during calibration. In Section VI, the technique is compared with other approaches. This paper concludes with Section VII.

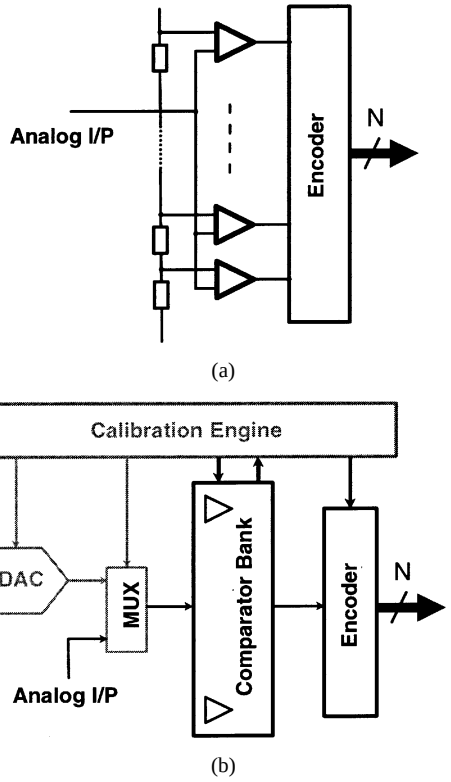

Fig. 1. (a) Traditional flash ADC. (b) Block diagram of a flash ADC calibrated with redundancy.

II. Overview of Digital Calibration With Redundancy

In a traditional N-bit flash ADC [see Fig. 1(a)], the input voltage is quantized by 2^N-1 comparators, with monotonically increasing, trip-voltages. The outputs of the comparators form a thermometer code that is encoded to give the N-bit output of the converter. A block diagram of the flash ADC with calibrated redundancy introduced by the authors in [8], is shown in Fig. 1(b). Instead of 2^N-1 comparators, the ADC has a bank of $R(2^N-1)$ comparators, with R comparators assigned to each

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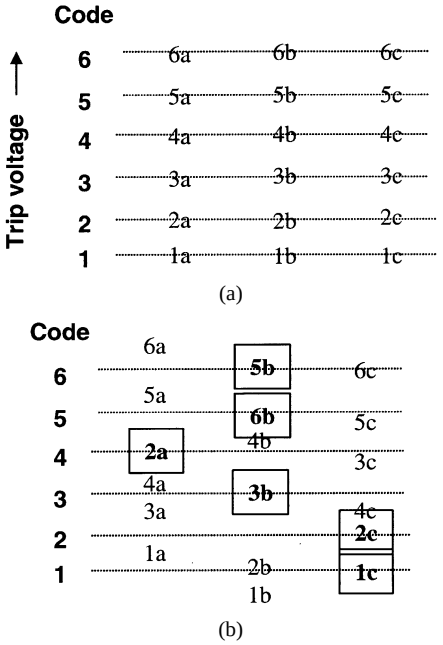


Fig. 2. (a) Nominal trip-voltages of comparators. (b) Example of the actual trip-voltages. The comparators that are selected during calibration are highlighted.

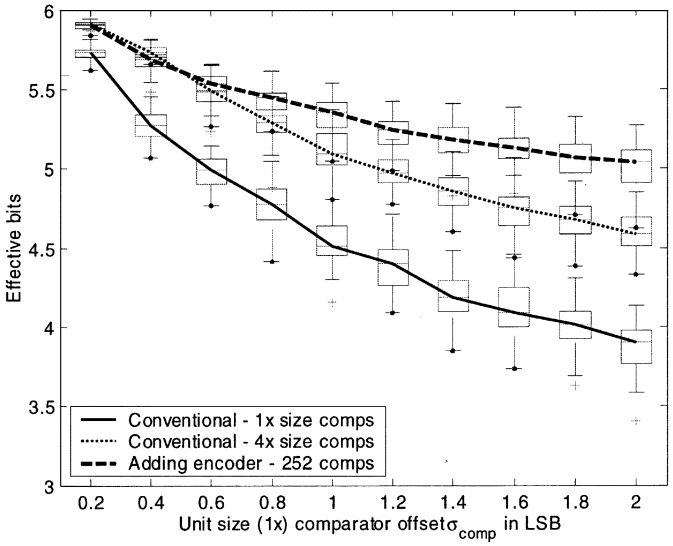


Fig. 3. This plot compares simulated effective resolution versus comparator offset for three different 6-bit flash ADC configurations: a conventional ADC with voting correction, a conventional ADC with 4× larger comparators (i.e., the effective sigma is halved), and an ADC with four comparators per code and with an adding encoder. The box plots indicate the median effective resolution and distribution.

code. During a calibration sequence at power-on, a finite state machine (the *calibration engine*) directs the search of the entire bank of comparators for the most suitable comparator for each code. Throughout this search, the resistor ladder is configured as a resistor DAC and generates test input voltages to the comparators. During calibration, a MUX connects the output of the resistor ladder DAC to the input of the comparator bank, while in normal operation, the ADC analog input is connected to the comparators.

Fig. 2 shows an example with R equal to 3. Fig. 2(a) shows the nominal trip-voltages with the trip-voltage of each of the R comparators for each code at the ideal value.[1] In practice, the comparator trip-voltages differ from the ideal trip-voltages because of offsets caused by device mismatch. Fig. 2(b) shows an example of actual comparator trip-voltages. The trip-voltages of the comparators that are selected from the bank of comparators are highlighted. For example, comparator $1c$ is chosen to represent code 1, and comparator $3b$ represents code 3. It should be noted that a comparator may be selected to identify a code other than the one associated with its nominal trip-voltage. To illustrate this, again referring to the example in Fig. 2(b), we see that comparator $2a$ is reassigned to represent code 4. Comparator *reassignment* is an important part of the overall technique.

Once the calibration phase is complete and normal operation begins, the comparators which have not been assigned are powered down. Therefore, as with a conventional flash ADC only $2^N - 1$ comparators are active. Because the technique overcomes the effect of large comparator offset, the comparators can be designed without consideration of offset. In practice, this means that small, fast transistors can be used. We will see that even allowing for redundancy, the total comparator area is less than with other techniques.

Since comparators can be reassigned, the comparator outputs do not form a thermometer code as in a traditional flash ADC. It is impossible to predict how the comparators are reassigned; therefore, traditional encoders that find the "top" of a thermometer code can not be used. Instead we count (i.e., add) the comparator outputs that are equal to 1, to generate the conversion result. A counting encoder has a number of significant advantages in this scheme. Reassignment is handled automatically because unlike a thermometer encoder, a counting encoder does not associate comparators with codes. If a comparator is chosen for a code, it is simply enabled. Disabled, unselected comparators always generate a 0 output and so do not influence the result.

To summarize, $2^N - 1$ comparators are chosen from a bank of $R(2^N - 1)$ redundant comparators. Comparators may be reassigned to represent codes other than those associated with their nominal trip-voltages. A counting encoder is well suited to the scheme and handles comparator reassignment transparently.

III. Why Is the Scheme Attractive?

In order to gain a better understanding of how the scheme works, we explore some alternatives based on comparator size and on averaging. Later we compare these alternatives with calibrated redundancy. From these experiments we will see the benefits of comparator *reassignment* and *selection*. We use Monte Carlo simulations to investigate 6-bit implementations of these schemes; however, our observations are also valid for higher resolution ADCs.

Fig. 3 shows simulation results for three different 6-bit flash ADC configurations. The standard deviation of comparator offset (σ_{comp} is swept from 0.2 to 2.0 *LSB*, and for each value of σ_{comp} the distribution and the median value of effective

[1]In this example all redundant comparators have the same nominal trip-voltage for each code. We could also distribute the nominal trip-voltages around the ideal value—this is helpful if there are nonuniform systematic comparator offsets.

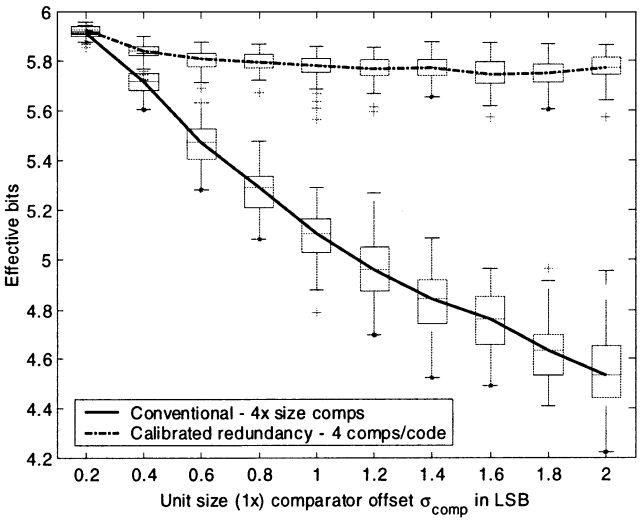
resolution are indicated. (The effective resolution is calculated from the signal-to-noise-and-distortion found through simulation [10]. Fifty ADCs are simulated for each value of σ_{comp}.) In this figure, the two traces marked *conventional* (i.e., 1× and 4× comparator area) indicate traditional flash ADCs with voting bubble error correction [11]. Since device mismatch is responsible for offset, and since mismatch is inversely related to square root of device area [12], we assume that the standard deviation of comparator offset of the larger 4× comparators is one half that of the 1× size comparators. As expected, the median effective resolution is higher in the 4× case.

Before we analyze the benefits of redundancy, it is instructive to first consider a scheme with extra comparators, but where these are not used in a redundant fashion. In other words, all comparators are enabled, and all contribute to the output. The third set of data presented in Fig. 3 (*adding encoder*) relates to a 6-bit ADC with 252 comparators (i.e., no selection). In this ADC, 4 nominally identical, 1× sized comparators are assigned to each code. A 6-bit ADC output is achieved by adding the outputs (i.e., counting the 1's) of all 252 comparators, dividing the result by 4, and rounding to the nearest integer.

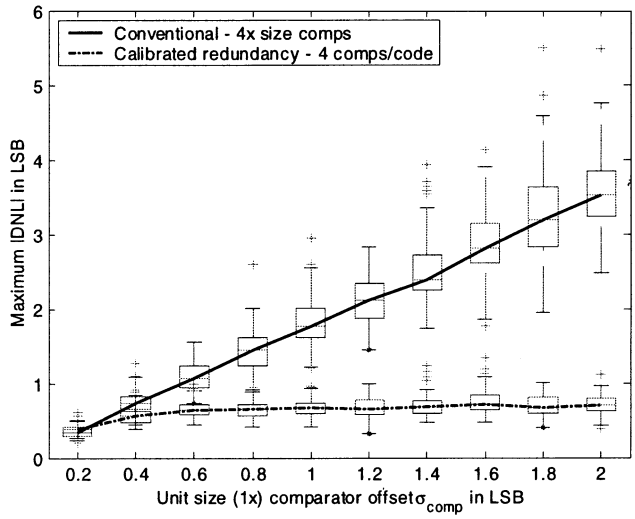
Intuitively, we would expect this averaging to produce a more accurate result. And in fact, we see from the figure that the median effective resolution is considerably higher than that of the conventional ADC comprised of 63 1× sized comparators. However, it is more meaningful to compare this ADC with the conventional ADC comprised of 4× sized comparators, since this has the same overall comparator area. For higher values of σ_{comp}, the 252 comparator ADC has a significantly better effective resolution; for example with σ_{comp} equal to 2 *LSB* the effective resolution is 0.5 bits higher.[2] This improvement is due to comparator *reassignment*—comparators with large offsets may better represent codes that differ from the nominal code. Unlike other flash ADC encoding techniques (i.e., those that identify the "top" of the thermometer code), addition does not require information on how the comparators are assigned, and therefore reassignment happens transparently. As we mentioned earlier, *reassignment* is one of the key features of the calibrated redundancy scheme.

It is the *selection* of comparators from the bank of redundant devices that dramatically improves the resilience to offset, and that makes the calibrated redundancy scheme attractive. When $2^N - 1$ comparators are selected from the bank of $R(2^N - 1)$, additional information is introduced that improves the quality of the ADC. For each code, the comparator with the most appropriate trip-voltage is selected. We can also view this process as removing, or pruning, the erroneous information provided by the $(R-1)(2^N-1)$ excluded comparators. We will see that with sufficient redundancy, good effective resolution is achieved even in the case of very large comparator offsets. Fig. 4(a) shows the variation of effective resolution versus σ_{comp} in the case of a 6-bit ADC with 63 comparators selected from 252. For comparison, the effective resolution of the conventional ADC of the same area from Fig. 3 is also shown. At σ_{comp} equal to *2 LSB*, the ADC with calibrated redundancy has an effective resolution less than 0.3 bits from ideal; this is more than 1.2 effective bits better than the equal area conventional scheme. Fig. 4(b) shows that use of redundancy significantly reduces differential nonlinearity (DNL).

[2]At low values of σ_{comp} the effective resolution of the conventional ADC of equal area is marginally better (by less than 0.03 effective bits). This slight difference is due to quantization, since in the 252 comparator ADC we are averaging digital values.



(a)



(b)

Fig. 4. Comparison of 6-bit ADC with calibrated redundancy (i.e., reassignment and selection) with a conventional ADC of the same area. (a) Diagram shows the effective resolution while (b) compares the worst case DNL.

IV. Analysis

In this section, we develop expressions for the yield of an ADC with calibrated redundancy. We use an approach similar to that applied by Pelgrom *et al.* in their analysis of a conventional flash ADC [1]. We first consider nonmonotonicity. Ideally, the comparator trip-voltages range from $V_{\text{trp\_ideal},\,1}$, the minimum trip-voltage, increasing in *1 LSB* steps to $V_{\text{trp\_ideal},\,2^N-1}$. In practice, the actual trip-voltages differ from the ideal values. If we assume the error in the trip-voltage has a Gaussian distribution then we can say

$$V_{\text{trp}P,\,j} = V_{\text{trp\_ideal},\,j} + \varepsilon, \qquad \text{where } \varepsilon \sim N(0,\,\sigma_{\text{comp}}). \quad (1)$$

In a conventional flash ADC, nonmonotonicity occurs when two comparator trip-voltages are interchanged, or in algebraic terms when $V_{trp,\,j+1} < V_{\mathrm{trp},\,j}$. (Ideally, $V_{\mathrm{trp},\,j+1} = V_{\mathrm{trp},\,j} + LSB$.) If p is the probability that two adjacent comparators become interchanged, or

$$p = P(V_{\mathrm{trp},\,i+1} < V_{\mathrm{trp},\,i}) \tag{2}$$

then the yield is the probability that none of the $2^N - 2$ pairs of the adjacent comparators are interchanged:

$$\mathrm{Yield} = (1-p)^{2^N-2}. \tag{3}$$

With the calibrated redundancy scheme, since comparators are reassigned, the effective trip-voltages cannot become interchanged because of offset. In other words, the yield as defined by the absence of nonmonotonicity, is always 100%.

In a more strict definition of yield, we define a good ADC as one with a maximum absolute value of DNL less than a certain value. As before, we begin with a conventional flash ADC. Ideally, the difference between the trip-voltages of adjacent comparators is *1 LSB*. For a particular code j, the DNL can be defined as

$$DNL_j = V_{trp,\,j+1} - V_{trp,\,j} - LSB. \tag{4}$$

If we specify a maximum allowable DNL, ($DNL_{\max}$) then the probability p of exceeding $DNL_{\max}$ at a particular code can be written as

$$p = P(|V_{\mathrm{trp},\,j+1} - V_{\mathrm{trp},\,j} - LSB| > DML_{\max}). \tag{5}$$

If a maximum DNL in excess of *1 LSB* can be tolerated, then this equation must be reformulated to preclude missing codes and nonmonotonicity

$$p = P(V_{\mathrm{trp},\,j+1} - V_{trp,\,j} - \mathrm{LSB} > \mathrm{DNL}_{\max}) + P(V_{\mathrm{trp},\,j+1} < V_{\mathrm{trp},\,j}). \tag{6}$$

The probability that the DNL is not excessive is $1 - p$. DNL is defined between the $2^N - 2$ pairs of trip-voltages, so the probability that the ADC is good is

$$\mathrm{Yield} = (1-p)^{2^N-2}. \tag{7}$$

This definition of a good ADC specifies both the maximum and minimum values of DNL. On the other hand the absence of missing codes and nonmonotonicity only requires that minimum DNL be greater than *−1 LSB*.

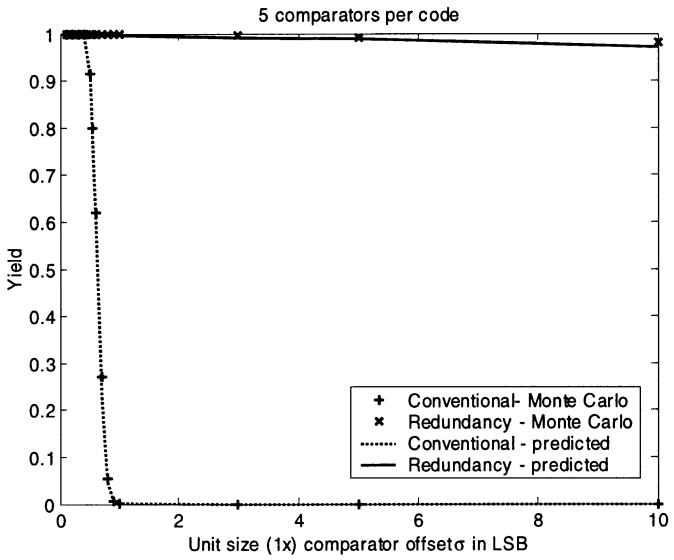
We now derive a similar formulation of yield for an ADC with calibrated redundancy. We first consider an ADC without redundancy. As seen earlier, reassignment is achieved simply by using a *counting* encoder. (We consider redundancy later.) Let $V_{x,\,k}$ where $k = 1 \cdots 2^N - 1$, denote the actual trip-voltages of the $2^N - 1$ comparators. If the error in the trip-voltage has a Gaussian distribution then we can say

$$V_{x,\,k} = V_{\mathrm{trp\_ideal},\,k} + \varepsilon, \qquad \text{where } \varepsilon \sim N(0,\, \sigma_{\mathrm{comp}}). \tag{8}$$

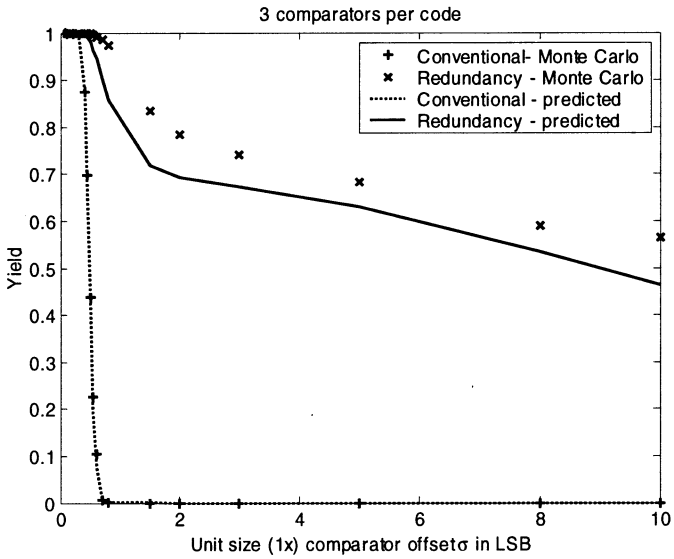
Because of random comparator offsets, the actual trip-voltages will not be uniformly spaced and may not increase monotonically. During reassignment, the comparators are reorganized in a monotonic series $V_{r,\,j}$ where $j = 1 \cdots 2^N - 1$. Ideally, the elements of V_r are spaced in *1 LSB* increments, that is $V_{r,\,j+1} - V_{r,\,j} = LSB$. The probability of excessive DNL is the probability of *not* finding an element of V_x within $1\,LSB \pm \mathrm{DNL}_{\max}$ above $V_{x,\,k}$. If comparators are assigned beginning with code 1, and we note that the set of available trip-voltages becomes smaller with increasing code, then an estimate for the probability p of not finding an element within the DNL range is given by

$$P_k = \prod_{i>k}^{2^N-1} P(|V_{x,\,i} - V_{x,\,k} - 1\,LSB| > \mathrm{DNL}_{\max}). \tag{9}$$

This equation is the product of the probabilities that each of the trip-voltages (other than $V_{x,\,k}$) does not meet our yield criterion, and assumes that codes less than k have already been assigned



(a)



(b)

Fig. 5. (a) and (b) compare the predicted yield with that found through Monte Carlo analysis for five and three comparators per code. The yield of a conventional 6-bit ADC of the same total comparator area is also shown for both cases. A good ADC has DNL values between *−1 LSB* and *1 LSB*.

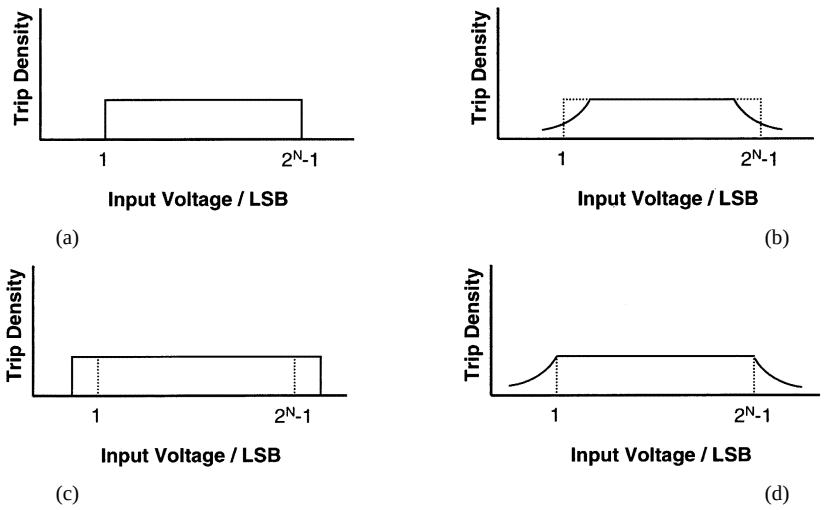


Fig. 6. (a) Nominal and (b) actual density of trip-voltages versus input voltage. (c) Nominal and (d) actual density of trip-voltages when extra comparators are added with nominal trip-voltages outside the ADC input voltage range.

trip-voltages. If $\mathrm{DNL}_{\max} > 1\ LSB$ is tolerated then this equation is rewritten to exclude nonmonotonicity and missing codes:

$$p_k = \prod_{i>k}^{2^N-1} P(V_{x,i} - V_{x,k} - 1\,LSB > \mathrm{DNL}_{\max}) + P(V_{x,i} - V_{x,k} < 0). \quad (10)$$

The probability that the overall ADC is good is estimated as:

$$\mathrm{Yield} = \prod_{k=1}^{2^N-2} (1 - p_k). \quad (11)$$

Here p is much smaller than for a conventional ADC, since comparators can be assigned to any code.

If redundancy is introduced, then the probability of *not* finding a trip-voltage within the tolerated range of DNL values is reduced. If there are R comparators per code, then the probability p and the yield become:

$$p_k = \prod_{i<k}^{2^N-1} [P(|V_{x,i} - V_{x,k} - 1\,LSB| > \mathrm{DNL}_{\max})]^{R-1} \times \prod_{i>k}^{2^N-1} [P(|V_{x,i} - V_{x,k} - 1\,LSB| > \mathrm{DNL}_{\max})]^{R}$$

$$\mathrm{Yield} = \prod_{k=1}^{2^N-2} (1 - p_k). \quad (12)$$

This estimate accounts for trip-voltages that have already been allocated by assuming that fewer trip-voltages are unassigned for codes below k. This equation shows that redundancy further increases the yield over that of a conventional ADC.

Fig. 5 compares the yield predicted by equation (12) with the yield determined by Monte Carlo analysis. In this comparison, a good ADC has a worst case DNL greater than *−1 LSB* and less than *1 LSB*. These plots show that the prediction of yield is good over a range of redundancy values.

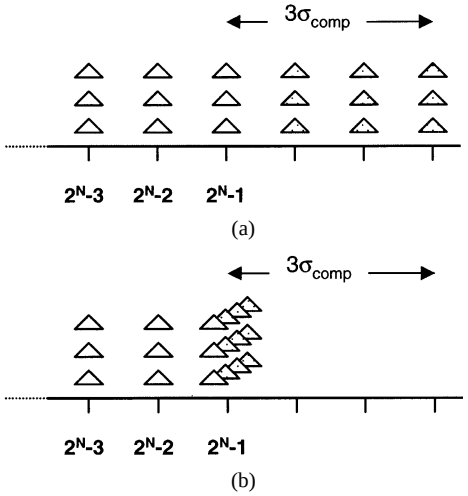


Fig. 7. (a) Extra comparators are added with trip-voltages past the nominal range of the ADC ($\sigma_{\mathrm{comp}} = 1$ LSB, 3 comparators per code), and (b) a more efficient use of the extra comparators.

V. Tradeoffs

A. Edge Effects

The calibrated redundancy scheme relies on probability, not accuracy, to achieve yield. It can only work if there is a good likelihood of finding comparator trip-voltages close to each code. We have seen that this likelihood is improved by adding redundant comparators. However, to find good trip-voltages over the entire ADC range, we also need to pay special attention to the edges of the range (i.e., near code 0 and code $2^N - 1$). To help understand this effect, in Fig. 6 we consider the *density of trip-voltages*, which we define as the number of tip-voltages located within a *1 LSB* range. Fig. 6(a) shows the density of nominal trip-voltages versus input voltage, while Fig. 6(b) is an example of the actual density of trip-voltages. The density of trip-voltages is low at the lowest and highest codes, since some of the trip-voltages have diffused past the range of the ADC. This makes it more difficult to find suitable comparators for low and high codes, reducing the yield of the ADC.

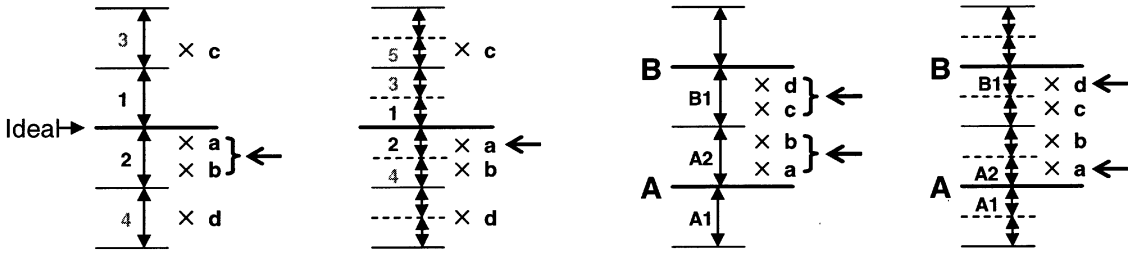


Fig. 8. (a) and (b) show the effect of DAC resolution on trip-voltage selection, while (c) and (d) show the relationship between DAC resolution and DNL.

Analogous edge effects occur in other analog circuits. For example, the end elements in a string of resistors, or in an array of capacitors, may not match well with the other elements. (Edge effects must also be considered in spatial averaging and interpolation schemes [4].) A common solution is to add dummy resistors around the periphery [13]. In a similar vein, in [9] we incorporate additional comparators with nominal trip-voltages outside the range of the ADC. In Fig. 6(c) and (d) we show the nominal and an example of actual densities of trip-voltages. Since the probability of a trip-voltage moving by more than $3\sigma_{\text{comp}}$ from the nominal value is less than 0.3%, extending the nominal ADC range by 3 σ_{comp} ensures an equally good likelihood of finding suitable comparators for mid-range and edge of range codes.

Fig. 7(a) shows how extra nominal comparator trip-voltages might be added. In this example, three comparators are assigned to each code. Since σ_{comp} is *1 LSB*, three sets of comparators at nominal increments of *1 LSB* are added. The additional trip-voltages can be used more efficiently if they are added within the nominal range of the ADC, as shown in Fig. 7(b). This modification increases the probability that the additional trip-voltages will lie within the ADC range.

B. DAC Accuracy

In addition to the distribution of trip-voltages, both the accuracy and resolution of the search DAC have a bearing on the overall accuracy of the ADC. During the calibration sequence, a DAC is used to search the space of comparator trip-voltages. The accuracy of this DAC should be at least equal to the desired accuracy of the ADC; however, the *resolution* of the DAC needs to be somewhat higher.

Fig. 8(a) shows one possible search sequence. (There are four trip-voltages marked a–d.) The search begins close to the ideal trip-voltage and moves outwards, until an unused trip-voltage is found. In this particular example the search stops at step 2 where two candidates are found: a and b. Since a and b are found in the same segment, there is no information to indicate that a is the more suitable trip-voltage, therefore, an arbitrary choice between a and b is made. Continuing with this example, we see that in (b), trip voltage a is selected when the size of the search segment is reduced, or in other words when the DAC resolution is increased.

Fig. 8(c) and (d) explain the relationship between search DAC resolution and DNL. Here A and B indicate the ideal trip voltages for two adjacent codes. Four actual comparator trip-voltages are identified a–d. In Fig. 8(c) the DAC resolution is 1 bit greater than the overall ADC resolution. The search for a trip-voltage close to A stops at step $A2$, finding two trip-voltages a and b, while the search for a trip-voltage close to B stops at step $B1$, finding c and d. Since there is no way of identifying the best trip voltages in a selected segment, the most suitable comparators may not be selected, resulting in a larger DNL. In Fig. 8(d) the DAC resolution is increased by one bit (i.e., now 2 bits above ADC resolution). Comparators a and d are now selected to represent A and B. A DAC resolution 2 bits higher than the ADC resolution is a good compromise between DAC complexity and ADC accuracy, since given the existence of suitable trip-voltages, the minimum and maximum DNL then are -0.5 and 0.5 *LSB*.

C. How Much Redundancy?

As we discussed in Section III, the yield of the ADC is a function of both comparator offset and redundancy. Once there is a certain amount of redundancy, the scheme is surprisingly resilient to comparator offset. This is illustrated by the Monte-Carlo simulation results presented in Fig. 9. In these simulations, a good ADC is defined as one with an effective resolution less than 0.5 bits from ideal. Fig. 9(a) and (b) show the variation in yield versus redundancy for 6- and 8-bit ADCs, for four values of comparator offset. We see that excellent yield is achieved with four or more comparators per code. Fig. 10(a) and (b) show the median loss in effective resolution under the same conditions.

VI. Comparison With Other Schemes

In this section, we compare calibrated redundancy with other techniques. Since for communications and other applications, fast flash ADCs must be implemented in the most advanced digital CMOS process, we also consider the effects of scaling. In Fig. 11, we group the techniques into three broad categories: 1) latching comparators without preamplifiers; 2) latching comparators with one or more stages of pre-amplification; and 3) trimmed latching comparators, possibly with trimmed preamplifiers.

A. No Preamplifier

Device sizing can be used to give stand-alone latching-comparators sufficient accuracy, but this approach is inefficient in terms of power and area. Calibrated redundancy breaks the link between comparator accuracy and ADC accuracy. The comparators can be built with fast, short devices, and as we have

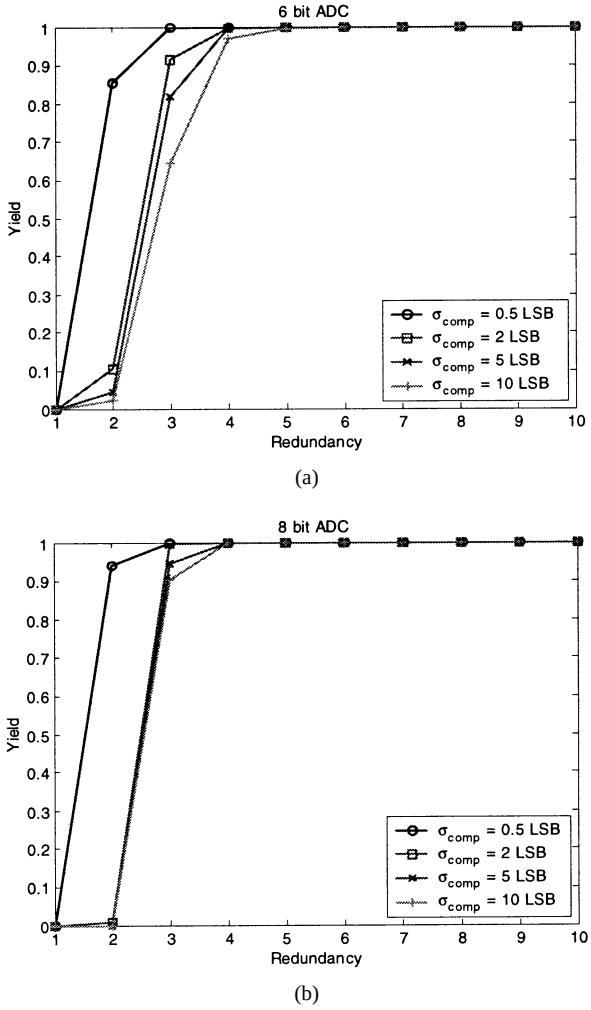


Fig. 9. Variation of yield with redundancy for (a) 6-bit and (b) 8-bit ADCs at four values of σ_{comp}.

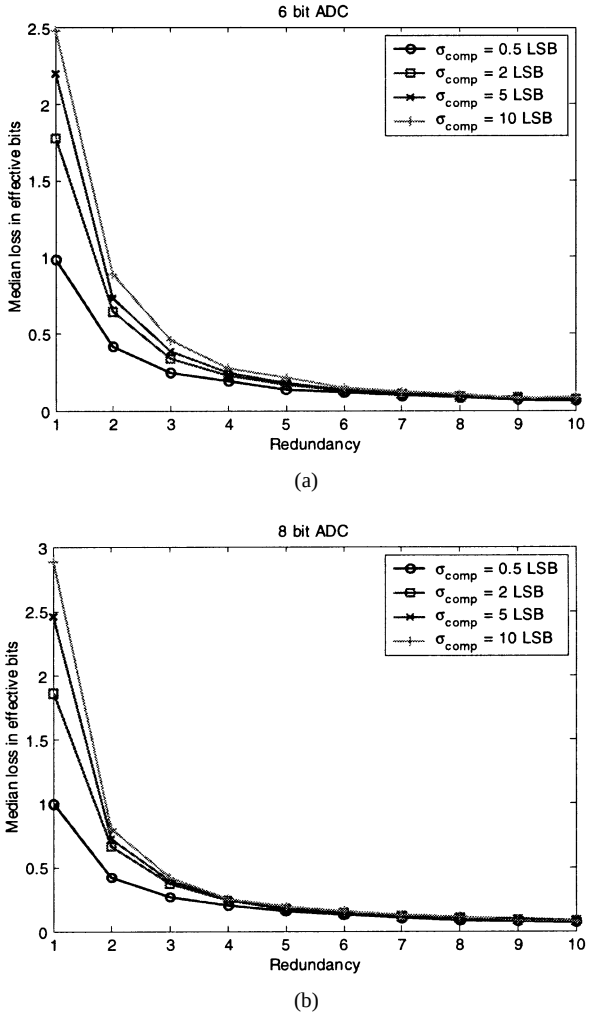


Fig. 10. Median effective loss in resolution versus redundancy for (a) 6-bit and (b) 8-bit ADCs.

seen, even accounting for redundancy, the overall comparator area is far smaller than with sizing. (This has power implications since power consumption is directly related to gate area [15].) For example using the approximation for yield derived in Section IV [see (5), (7), (9), and (11), and Fig. 5], with a redundancy of five comparators per code a yield of 98.9% is achieved with $\sigma_{\text{comp}} = 5\ LSB$, whereas a conventional ADC would need more than 120 times more comparator area to achieve the same yield.[3] The calibrated redundancy technique requires a calibration cycle at power-on, however, repeated calibration is not necessary [9], since transistor mismatch tends to be stable [12]. (Digital calibration of offsets at power-on is also shown to have long term stability in [14].)

B. Pre-Amplifier

In the second category, the input is pre-amplified to overcome the input offset of the latching comparator. The addition of a pre-amplifier moves the offset constraint from the latching comparator to the pre-amplification stage. This considerably relaxes the matching constraints in the design of the comparator, however the pre-amplifiers themselves must be designed to have low offset. Switched-capacitor techniques can be used to cancel pre-amplifier offset [2], [3]. In this way, amplifier offset is attenuated by amplifier gain. Because of switch and junction leakage, switched capacitor cancellation circuits must be refreshed at least every millisecond. Spatial filtering techniques [4], [5] do not require analog switches, and therefore, may be better suited to the low supply-voltage of deep-submicron processes. Interpolation distributes pre-amplifier offset reducing the overall ADC DNL [7]. Both interpolation and spatial filtering permit continuous operation.

We need more pre-amplification gain in more advanced processes if minimum length transistors are used. All pre-amplification techniques, including those that incorporate spatial filtering, must provide enough gain to overcome the offset of the latching comparator. The maximum allowed input-referred offset to achieve a certain yield of ADCs, where a good ADC has no missing codes, is given by equations (2) and (3). For example, for a 6 bit device to have a 95% yield (without nonmonotonicity), $\sigma_{\text{comp-input}}$ must be less than 0.23 *LSB*. The ratio of σ_{comp} to $\sigma_{\text{comp-input}}$ is the pre-amplification gain.

[3]In this example a comparator in the conventional ADC is 600 times larger than in the calibrated-redundancy case. Comparator power dissipation should also be approximately 600 times larger to achieve the same regenerative time constant (assuming same V_{GS}–V_T).

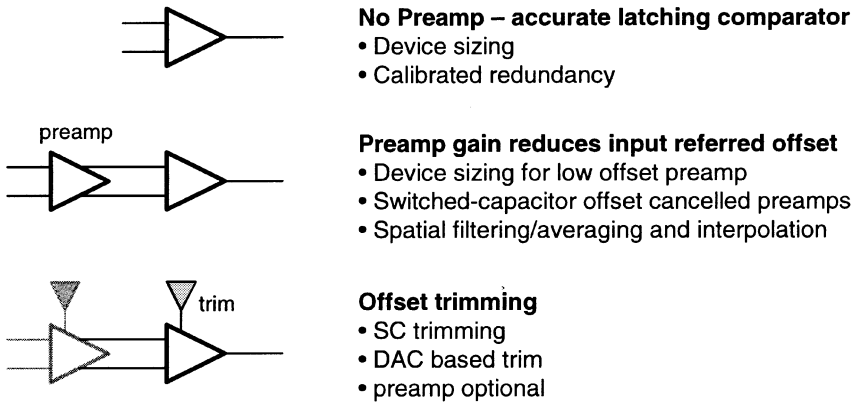


Fig. 11. Comparator offset control techniques.

If we assume $\sigma_{\rm comp}$ is proportional to threshold voltage offset [12], then

$$\sigma_{\rm comp} = K_{\rm comp}\frac{A_{Vt}}{\sqrt{WL}} \tag{13}$$

where, A_{Vt} is the process constant for matching, and $K_{\rm comp}$ is a constant related to the design of the comparator. If $K_{\rm comp}$ and the $W:L$ ratio are fixed, and $LSB = Vdd/(2^N - 1)$ then the required pre-amplification gain is:

$$\text{gain} \propto \frac{A_{Vt}}{L \cdot Vdd}. \tag{14}$$

Using the predictions of the ITRS for A_{Vt} [16], [17], in Fig. 12 we see that the normalized gain must increase significantly over the next few years, increasing the power consumption and complicating the design of the pre-amplifiers.

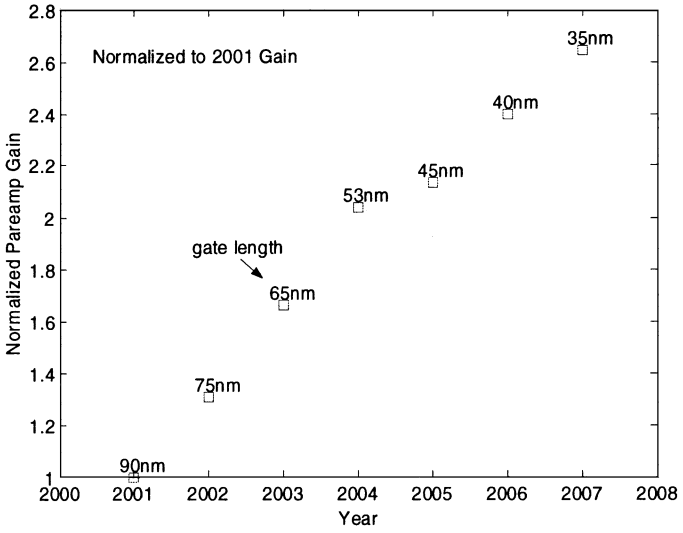


Fig. 12. Minimum normalized preamplifier gain based on ITRS predictions for gate length, A_{Vt} and Vdd. The minimum gate length is indicated for each technology node.

C. Trimming

The third category consists of comparators, which rely on trimming to ensure accuracy. In these schemes, a trim current (or voltage) is applied to cancel the offset of each latching comparator (or of a preamp). Pelgrom *et al.* [1] describe one analog trim technique. More recently, digitally controlled trim techniques have been presented [6]. The trim value for each comparator is stored in a register and converted to current (or voltage) with separate DACs. A calibration routine, initiated at power-up, programs the appropriate value in each register. The DAC LSB size is directly related to the required DNL. For example, the DAC LSB size should correspond to a *1 LSB* change in offset in order to achieve a $|\,\text{DNL}\,| < 1\,LSB$. The size of the register and the DAC resolution depend on the statistics of comparator offset and on the accuracy of the DAC. The range of the DAC depends on the variability of comparator offset and the required probability that the calibrated comparator offset should achieve a particular DNL (i.e., the yield). This probability p that the DAC range must accommodate the worst comparator offset is related to the required ADC yield

$$\text{Yield} = p^{2^N-2}. \tag{15}$$

For large values of $\sigma_{\rm comp}$ this scheme can have a significant analog and digital hardware overhead. For example, if we require a 6-bit ADC to have 99% yield, then p must be at least 0.9998. If we assume a Gaussian distribution for comparator offset, this implies a DAC range of $\pm 3.7\ \sigma_{\rm comp}$. If $\sigma_{\rm comp} = 3\,LSB$, and we want to calibrate to $|\text{DNL}| < 0.5\,LSB$, then each trim DAC should have a resolution of almost 6 bits.

VII. Conclusions

Calibrated redundancy is an attractive alternative to traditional flash ADC schemes particularly in deep-submicron CMOS. Since analog accuracy is traded for digital complexity, this scheme allows us to take advantage of the increasing speed of CMOS transistors. This paper presents an analysis of the scheme, examines some tradeoffs and presents a comparison with other schemes. We present a statistical analysis of ADC yield. This new analysis is verified through Monte Carlo simulation. Excellent yield is achieved with a redundancy or four or five comparators per code.

Acknowledgment

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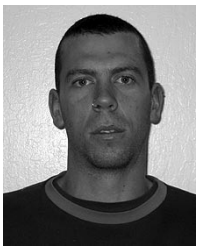

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