Brief Papers

A "Digital" 6-bit ADC in 0.25-μm CMOS

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***Abstract*—Traditionally, circuit designers have adopted analog techniques to overcome comparator offset in flash converters. These schemes have an adverse effect on area and power consumption and, more seriously, do not scale easily to low-voltage processes. We describe a digital technique which removes the accuracy constraints from the comparators. With no analog matching requirements, the comparators can be small, fast, and power efficient. A 6-bit prototype converter built in a standard 0.25-μm digital CMOS process occupies 1.2 mm^2 and dissipates 150 mW from a 2.2-V supply at 400 MS/s.**

***Index Terms*—Analog-to-digital converters, CMOS analog integrated circuits, data converters, digital calibration.**

I. Introduction

THE TREND toward increased integration of analog and digital circuitry requires that data converters be embedded in large digital ICs. Mixed-signal applications such as partial-response maximum-likelihood (PRML) read channels and Gigabit ethernet require high-speed low-resolution ADCs which are usually implemented with the flash architecture. By their nature, these applications rely heavily on DSP, which performs best when implemented on the finest geometry CMOS process. On the other hand, ADCs, as with analog circuits in general, tend to function best when fabricated on more mature CMOS or BiCMOS processes.

Comparators are the key analog building block of any flash ADC and strongly influence performance. A high degree of comparator accuracy is essential for good ADC performance. However, integration of analog circuitry in low-voltage scaled VLSI technologies results in degraded precision due to large device mismatch and limited voltage swing. Reduced precision can be compensated for through the use of offset correction schemes. Analog offset correction techniques are typically used, but these schemes are increasingly difficult to implement in modern CMOS processes. For this reason, the issue of comparator offset is becoming a bottleneck in the design of flash ADCs.

This work focuses on reducing the amount of analog design and analog circuitry in a flash ADC. In particular, a flash ADC scheme was developed which tolerates low precision comparators. Much of the signal processing within the ADC has been transferred from the analog domain to the digital domain. In essence, digital techniques are used to compensate for the analog non-idealites. This alleviates the problem of difficult analog design, while harnessing the enhanced performance of digital circuits. The remaining analog components have "digital" accuracy requirements.

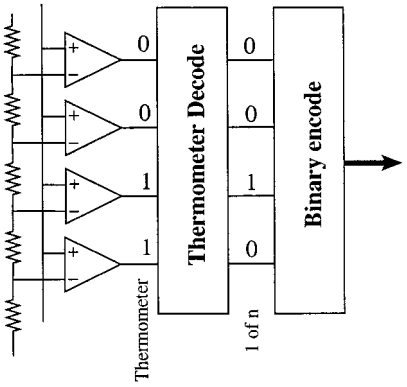

Fig. 1. Conventional flash ADC.

Because of the relaxed matching requirements, the comparators are small, fast, and power efficient. Comparator reassignment and redundancy are key features of this scheme. On power-up, a calibration cycle is executed. Once this is complete, continuous conversion is possible.

Some common analog offset correction approaches are described in Section II. A digital calibration scheme is introduced in Section III. Section IV discusses redundancy levels. Section V describes the ADC architecture. Measured results are presented in Section VI. Finally, a conclusion is given in Section VII.

II. Offset Correction

A block diagram of a traditional flash ADC is shown in Fig. 1. An N-bit converter has $2^N - 1$ comparators. The nominal trip-point of each comparator is set by a resistor ladder. Ideally, the comparator outputs form a thermometer code. The position of the meniscus (i.e., the 1–0 transition) represents the analog input and is determined by a thermometer decode circuit. The thermometer decode block generates a "1 of n" code which is converted to binary.

In practice, there may be random or systematic offsets in the comparator trip-points. Offsets introduce differential non-linear (DNL) errors and more seriously can cause non-monotonicity.

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Non-monotonicity occurs when the trip-points of adjacent comparators are interchanged. Bubbles or sparkles can be introduced in the thermometer code, causing serious degradation of the ADC linearity and signal-to-noise-plus-distortion ratio (SNDR) [1], [2].

Achieving monotonicity while maintaining acceptable yields dictates that offsets be tightly controlled [3]. To reliably achieve monotonicity necessitates that [3]

$$\sigma_{\text{offset}} < 1/4\,\text{LSB} \tag{1}$$

where σ_{offset} is the standard deviation of random comparator offset.

Achieving good linearity (i.e., $\text{DNL} < 0.5$ LSB), places higher demands [3]:

$$\sigma_{\text{offset}} < 1/8\,\text{LSB}. \tag{2}$$

For a 6-bit ADC in modern CMOS processes, this requires that σ_{offset} be no more than a few millivolts. Several techniques have been used to reduce comparator offsets to this level.

Large transistors may be employed, reducing the transistor mismatch [3]. However, the power and area overheads can be considerable. Increased input capacitance is another disadvantage of using large input transistors.

In [4], [5], the input to each comparator is pre-amplified, reducing the matching requirements of the comparator. In these schemes, switched capacitor techniques are used to cancel the pre-amplifier offset. However the pre-amplifiers consume power and area. Moreover, the pre-amplifier offset must be refreshed on storage capacitors periodically (approximately every 100 μs), preventing continuous conversion. Some applications, for example, hard disk drive read channels, allow discontinuous conversion, while others do not. In addition, switched capacitor techniques require considerable analog design effort and are difficult to implement in low voltage processes.

In [6], a trimming DAC current is used to reduce the offset. A more complex comparator architecture is employed, increasing the analog design effort.

With these analog approaches to offset reduction, minimization of comparator power and area is not possible. Furthermore, they increase the analog complexity.

III. Digital Offset Calibration

The offset calibration approach devised in this work places an emphasis on digital circuitry. Large random offsets are allowed, enabling comparators to be fast, while consuming minimal power and area.

To introduce the offset calibration scheme, we consider the comparator trip-point distributions given in Fig. 2. Fig. 2(a) shows an ideal ADC, in which comparators have zero offset. The converter has no DNL errors and perfect linearity. In Fig. 2(b), large comparator offsets have caused the trip-points of comparators 4 and 5 to become interchanged. The sequence of trip-points is no longer monotonic. If basic encoding schemes are used, a missing code and discontinuity are seen at the ADC output. This causes large DNL errors and serious linearity degradation.

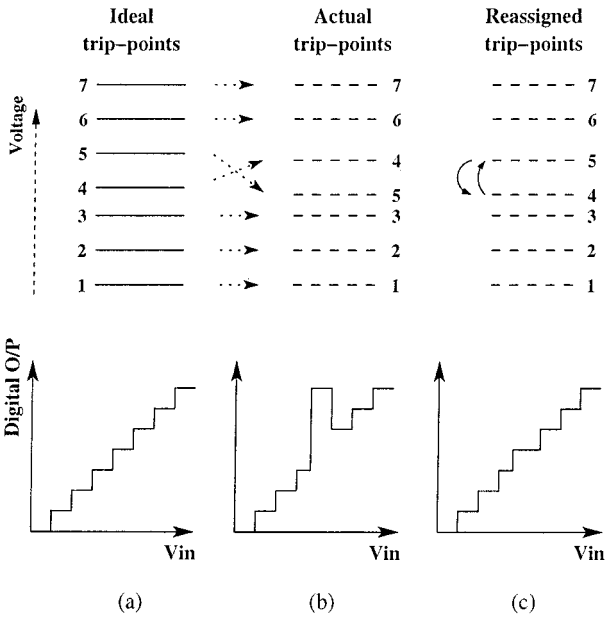

Fig. 2. Trip-points. (a) Ideal. (b) Actual. (c) Reassigned.

A. Comparator Reassignment

Non-monotonicity within the trip-point set can be corrected by reassigning comparators. In Fig. 2(c), comparator 5 is reassigned to represent code 4, while comparator 4 is reassigned to represent code 5. The DNL errors are reduced significantly and the missing code is eliminated. The technique of reassignment inherently ensures monotonicity, regardless of the offset magnitude. However, although reassignment guarantees monotonicity without the offset constraints of (1), most applications also require good linearity.

B. Comparator Redundancy

Comparator reassignment ensures monotonicity, however, large DNL errors may still exist. Redundancy is used in conjuction with reassignment to reduce DNL errors. Redundancy involves assigning more than one comparator to each code. This increases the probability of finding a comparator close to each ideal trip-point. A search is performed to find the trip-point nearest to each ideal threshold. The comparators closest to each code are then used for conversion, while the remaining comparators are ignored and powered down.

To demonstrate redundancy, consider the trip-point distributions shown in Fig. 3. In this case, three comparators are assigned to each code (i.e., comparators 3a, 3b, and 3c are nominally assigned to code 3). Ignoring redundancy and considering only comparators $1a \rightarrow 5a$ in the actual case [see Fig. 3(b)], we see that the trip-point distribution is uneven, causing significant DNL errors.

Incorporating redundancy [i.e., now considering all trip-points in Fig. 3(b)], we see that there is an actual trip-point near every ideal trip-voltage. Comparators 1b, 5a, 1c, 4b, and 1a form a set of well-distributed trip-points, and result in low DNL errors. In general, by employing sufficient redundancy, a trip-point can be found sufficiently close to each ideal

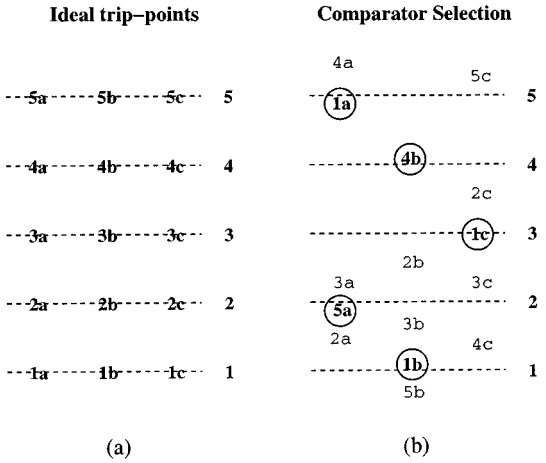

Fig. 3. Comparator redundancy and reassignment. (a) Nominal trip-points. (b) Example of actual comparators with offsets.

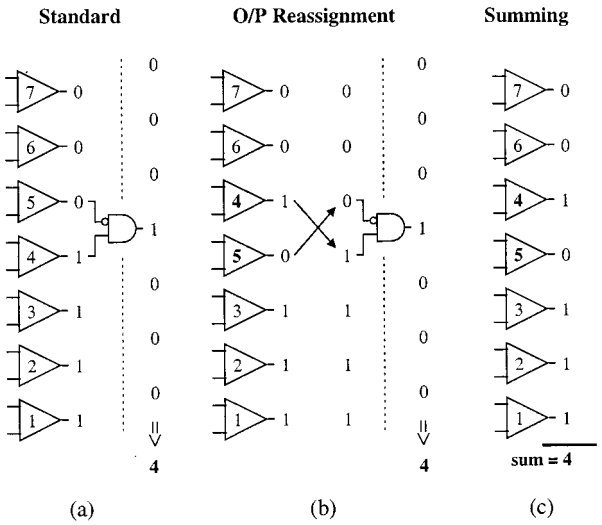

Fig. 4. Encoder solutions. (a) Standard encoder. (b) Output reassignment. (c) Summing.

trip-voltage. Selecting these trip-points results in a good trip-point distribution, and good linearity.

C. Comparator Selection

At power-up, a calibration sequence is executed. During this cycle, the comparator with a trip-point closest to the ideal threshold is selected for each code. Again considering Fig. 3(b), comparator 1b has a small offset. Its trip-point is the nearest to code 1, and it is selected for code 1. Although comparator 5a has an offset $\simeq$ 3 LSBs, its trip-point is the nearest to code 2 and it is selected for code 2. Comparator 1c has an offset $\simeq$ 2 LSBs. However, its trip-point is the nearest to code 3 and it is selected for code 3.

Even though a comparator may have a large offset (several LSBs), it can still be assigned to a code. This contrasts with traditional flash ADCs which require every comparator to have low offset in order to achieve good performance. With this approach, good ADC performance depends upon having a trip-point in close proximity to each code. Matching of individual comparators is not a prerequisite. Because a comparator may potentially be assigned to any code, the use of comparators is far more efficient.

During the calibration phase, $2^N - 1$ comparators are chosen. The unselected comparators are powered down, therefore, redundancy does not increase power. The calibration scheme breaks the link between comparator matching and ADC performance, so the power should reduce as the design scales to finer processes. The comparators have low offset requirements, enabling small devices to be used throughout. This results in small comparator area. For this reason, comparator redundancy presents little area overhead.

D. Encoder

Although the new calibration technique simplifies comparator design, additional demands are placed on the encoder. The encoder must account and compensate for the following.

- Reassignment of comparators to other codes is employed—any comparator can be assigned to any code.
- Only a subset of the comparator outputs are valid. Unselected comparator outputs must be ignored.
- The comparator outputs no longer form a thermometer code.

Traditional ROM-type encoders are not capable of processing such an unwieldy set of comparator outputs. Fig. 4 illustrates some encoder solutions. In Fig. 4(a), no comparator reassignment has taken place and a traditional encoder architecture may be used.

In Fig. 4(b), the trip-points of comparators 4 and 5 are interchanged. There is a bubble in the comparator outputs. To correct for this, comparators 4 and 5 can be reassigned. A possible solution in this case is to explicitly reassign the comparator outputs to form a thermometer code—as in Fig. 4(b). A traditional encoder may then be used to complete the encoding process. This approach requires a large switching matrix which has large area and power requirements.

A summing encoder is used in [7], to give maximum immunity to thermometer code bubbles. A summing encoder can also be used in this flash ADC topology. The correct digital output is derived by summing the comparator outputs, as shown in Fig. 4(c). This encoder architecture must account for comparator redundancy and reassignment. With redundancy, the outputs of unselected comparators must be ignored. In this implementation, unselected comparators have a default output of 0, and do not contribute to the summed result, so comparator redundancy is easily accommodated. A summing encoder implicity handles comparator reassignment. Due to the ease of operation, a summing encoder topology was selected.

IV. Trip-Point Distribution

The success of this scheme depends upon finding a trip-point in close proximity to each ideal code threshold. This is achieved by ensuring an even distribution of trip-points across the ADC input range.

A. Degree of Redundancy

In order to achieve good performance, a sufficient amount of comparator redundancy must be incorporated. To assist in the analysis, a MATLAB model of the ADC was developed to

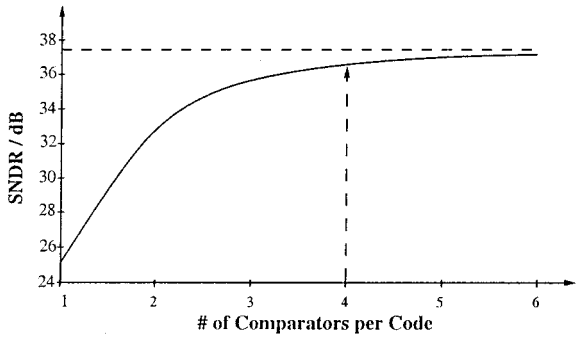

Fig. 5. Variation of SNDR versus redundancy (from simulation).

perform Monte Carlo simulations. Fig. 5 shows the variation of mean SNDR versus comparator redundancy for a 6-bit ADC. The SNDR tends to the ideal SNDR as the redundancy is increased. For a 6-bit ADC, a redundancy of four comparators per code gives a mean SNDR figure of 36.8 dB. As redundancy is increased beyond four comparators per code, the improvement in ADC performance is negligible. In the simulation, comparators are allowed have a large random offset of

$$\sigma_{\text{offset}} = 5\,\text{LSB}. \tag{3}$$

This is significantly larger (approximately 40 times greater) than the offset magnitude tolerated by traditional flash ADCs. This calibration scheme merely requires that comparators have "digital" precision.

B. Edges of the Input Range

An even distribution of trip-points across the full input range is necessary for optimal ADC performance. In the ideal case [shown in Fig. 6(a)], the trip-point density is uniform across the input range. In the actual case, [shown in Fig. 6(b)], some trip-points nominally assigned to codes near the input range edges may occur outside the input range edges (due to random offsets). This effect can be thought of as being similar to diffusion. This reduces the trip-point density at the input range edges, making it more difficult to find suitable trip-points in these regions, thus resulting in larger DNL errors at these codes.

To solve this problem, extra references are included beyond the input range edges. The effect of this can be observed in Fig. 6(c). The density of trip-points across the input range is now uniform. Simulations indicate that it is sufficient to add ten extra references beyond the input range. Hence, the total number of ADC references is $10 + 63 + 10 = 83$.

V. ADC Architecture

A block diagram of the converter is shown in Fig. 7. In addition to the comparators and encoder of a standard flash, the ADC employs a calibration engine, DAC, and an analog multiplexor (MUX).

A. DAC

During comparator selection, dc voltages are applied to the comparator inputs. This function is performed by the DAC. An analog MUX switches the input to the comparators between the

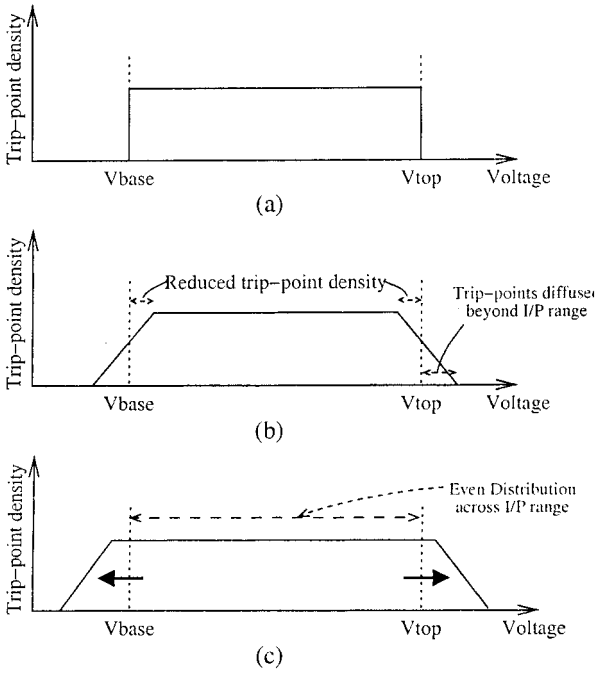

Fig. 6. Trip-point distribution over the input range. (a) Ideal case. (b) Actual case. (c) Actual case (extended ladder).

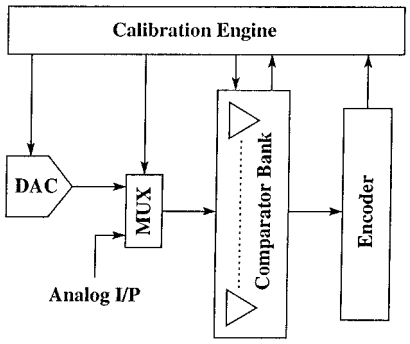

Fig. 7. ADC architecture.

DAC output and the ADC input. During calibration, the DAC output is fed to the comparators, while during the normal conversion phase, the DAC is idle. The DAC employs a resistor ladder architecture, using the same resistor ladder which provides the reference levels for the comparators.

B. Calibration Engine

A calibration cycle controlled by the calibration engine is executed at power-up. During a particular comparator search, the calibration engine adjusts the DAC output to find the comparator trip-point nearest the ideal threshold. The calibration engine is comprised of approximately 1000 standard cell gates and occupies an area of only 0.04 mm^2.

C. Comparator

A simple CMOS comparator [8] is employed. Due to the very low matching requirements, the comparator was optimized for maximum speed with minimum power and area. The layout area is equivalent to that of 1.5 D-type flip-flops and is approximately 20–30 times smaller than a traditional auto-zero comparator.

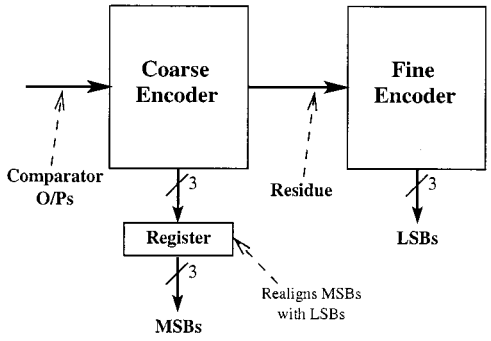

Fig. 8. Two-stage encoder block diagram.

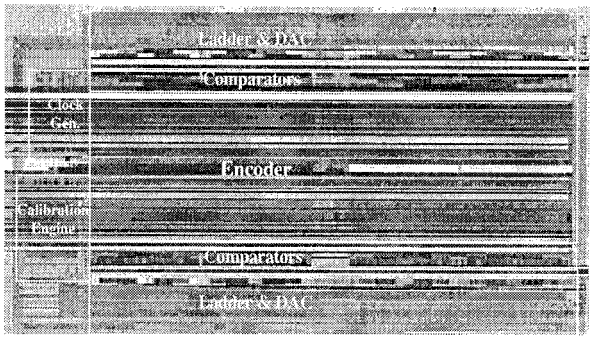

Fig. 9. Die photo.

TABLE I
MEASURED ADC CHARACTERISTICS

Resolution	6-bit
LSB size	15mV
Input Capacitance	1.2pF
Latency	2.5 clock cycles
Supply Voltage	2V ↔ 2.8V
Power @ 400MS/s	150mW
Area	1.2mm^2
Operating Temperature	−25°C ↔ 125°C
Process	0.25μm digital CMOS
Package	28-pin Ceramic LCC

D. Encoder

As discussed in Section III, a summing encoder is the preferred architecture for this ADC structure. Wallace-tree topologies [7] have been used to implement summing encoders for flash ADCs. However, the latency of such encoders can be quite high. To reduce the encoder latency, a two-stage counting encoder architecture was devised (see Fig. 8).

Operation of this encoder is analogous to the operation of a two-step ADC. The coarse stage determines the 3 MSBs and outputs a residue. The fine stage then uses the residue to determine the 3 LSBs. The latency of the encoder is two clock cycles.

VI. EXPERIMENTAL RESULTS

A 6-bit prototype ADC was fabricated in a 5-metal single-poly 0.25-μm digital CMOS process. The ADC core occupies 1.2 mm^2. A die photograph is shown in Fig. 9. Measured performance is summarized in Table I.

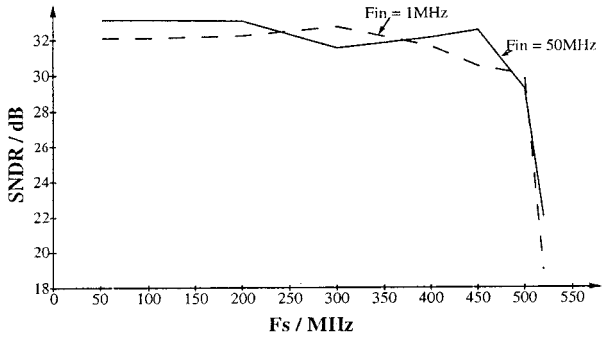

Fig. 10. Variation of SNDR with sampling frequency.

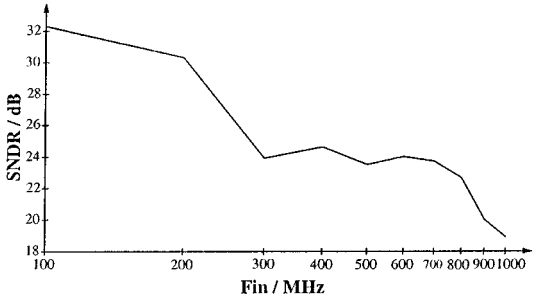

Fig. 11. Variation of SNDR with input frequency.

TABLE II
ADC COMPARISON

Author	Fs (MHz)	Speed/Power (mW/MHz)	Area (mm^2)
This work	**500**	**0.4**	**1.2**
Choi [10]	1300	0.42	0.8
Geelen [11]	1100	0.33	0.3
Nagaraj [5]	700	0.27	0.45
Sushihara [12]	800	0.5	1.7
Tamba [6]	500	0.8	2.4
Mehr [4]	500	0.75	0.8
Tsukamoto [13]	400	0.47	1.2

Fig. 10 shows the variation of SNDR with sampling frequency, for input frequencies of 1 MHz and 50 MHz. At lower sampling frequencies (<200 MS/s), SNDR is better than 33 dB. More than five effective bits are achieved up to a sampling frequency of 400 MS/s. As the sampling frequency increases beyond 500 MS/s, SNDR degrades significantly. This is due to the limited operation speed of the encoder. The deviation between the results predicted by simulation (SNDR = 36 dB) and actual results (SNDR = 33 dB) is due to a ladder layout problem, which causes large DNL errors at half-scale.

Fig. 11 shows the variation of SNDR versus input frequency for a sampling frequency of 300 MS/s. The SNDR degrades gracefully with frequency. At 400 MS/s, the converter dissipates 150 mW from a 2.2-V supply. Table II shows that the performance of this ADC is competitive with that of recently published conventional flash ADCs.

Over a 12-h period of continuous operation and without recalibration, the SNDR varied by less than 0.1 dB. To observe the variation of ADC performance over temperature, the ADC was calibrated at 25 °C. The operating temperature was then

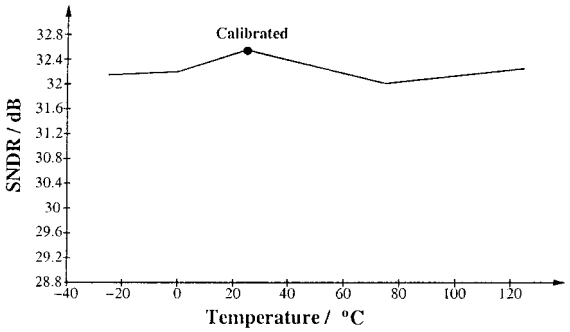

Fig. 12. Variation of SNDR with temperature.

swept up to 125 °C and down to −25 °C, without recalibration. Fig. 12 shows the observed variation of SNDR over temperature. SNDR varies by as little as 0.7 dB across the temperature range (temperature does not have a significant effect on transistor matching behavior [9]). All 20 parts tested are completely functional, achieving an SNDR of better than 32.4 dB.

VII. Conclusion

This digital calibration scheme removes the requirement for accurate comparators. Comparator redundancy and reassignment are used to achieve good performance, while introducing minimal overheads. Good ADC performance has been achieved at high conversion rates. The calibration technique breaks the link between comparator matching and performance. Digital techniques are used to compensate for analog non-idealities. Speed, power, and area of the ADC will scale in the same fashion as digital circuits. Low-voltage operation is facilitated. After initial calibration, the ADC can convert continuously without recalibration. The analog complexity is significantly reduced. Hence, porting the ADC to finer geometry processes is easier. The ADC topology is well suited for integration into mixed-mode ICs.

Acknowledgment

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