CMOS DLL-Based 2-V 3.2-ps Jitter 1-GHz Clock Synthesizer and Temperature-Compensated Tunable Oscillator

David J. Foley, *Student Member, IEEE,* and Michael P. Flynn, *Senior Member, IEEE*

***Abstract*—This paper describes a low-voltage low-jitter clock synthesizer and a temperature-compensated tunable oscillator. Both of these circuits employ a self-correcting delay-locked loop (DLL) which solves the problem of false locking associated with conventional DLLs. This DLL does not require the delay control voltage to be set on power-up; it can recover from missing reference clock pulses and, because the delay range is not restricted, it can accommodate a variable reference clock frequency. The DLL provides multiple clock phases that are combined to produce the desired output frequency for the synthesizer, and provides temperature-compensated biasing for the tunable oscillator. With a 2-V supply the measured rms jitter for the 1-GHz synthesizer output was 3.2 ps. With a 3.3-V supply, rms jitter of 3.1 ps was measured for a 1.6-GHz output. The tunable oscillator has a 1.8% frequency variation over an ambient temperature range from 0 °C to 85 °C. The circuits were fabricated on a generic 0.5-μm digital CMOS process.**

***Index Terms*—CMOS analog integrated circuits, delay-locked loops, frequency synthesizers, tunable oscillators, voltage controlled oscillators.**

I. Introduction

TRADITIONALLY, phase-locked loops (PLLs) have been used for clock synthesis. The synthesizer and tunable oscillator outlined in this paper employ a delay-locked loop (DLL). A DLL is more stable than higher order PLLs and requires only one capacitor in its first-order loop filter. On the other hand, a PLL generally requires a more complex second-order filter. This filter usually employs larger components which may need to be off chip. Additionally, a DLL offers better jitter performance than a PLL because phase errors induced by supply or substrate noise do not accumulate over many clock cycles [1].

The self-correcting DLL overcomes problems of false locking associated with conventional DLLs. A self-correcting circuit detects when the DLL is locked, or is attempting to lock, to an incorrect delay and then brings the DLL into a correct locked state. This DLL does not require the delay control voltage to be set on power-up; it can recover from missing reference clock pulses and, because the delay range is not restricted, it can accommodate a variable reference clock frequency. This paper describes how a small number of additional digital logic gates are required to convert a conventional DLL into a wider range self-correcting DLL. For comparison, in [2] a second DLL is added to achieve wider range operation.

The synthesizer outlined in this paper operates over a wide range of input reference clock frequencies and generates a low-jitter output clock running at nine times the reference frequency. Jitter measurements of 3.2 ps rms and 20 ps peak-to-peak, for a 2-V supply and 1-GHz output frequency, show that the core DLL compares well with recently reported DLLs [2], [3]. Multiple clock phases from the DLL are combined using digital logic to produce the synthesizer output [4]. An alternative approach requiring a pair of on-chip tuned *LC*-tanks is described in [5].

The tunable voltage-controlled oscillator (VCO) is intended for use in a transceiver where the receive and transmit clocks are plesiochronous. It is possible to tune the VCO around a center frequency while still maintaining good temperature independence. In some applications it may also act as a replacement for a fractional-N-type synthesizer. This circuit is similar to the oscillator described in [6] but it uses a lower jitter DLL in place of the PLL and can operate over a wider frequency range.

In Section II the DLL architecture is discussed, starting with a review of a conventional DLL and progressing to the new self-correcting architecture. Section III outlines the clock synthesizer architecture. This is followed in Section IV by an outline of the temperature-compensated tunable oscillator architecture. Section V discusses the circuit layout and Section VI introduces measured performance results for the two circuits. This paper then concludes in Section VII with a summary of the achievements of this work.

II. DLL Architecture

A. Conventional DLL

A simplified block diagram of a conventional DLL is illustrated in Fig. 1. This circuit contains a voltage-controlled delay line (VCDL), a phase detector, a charge pump, and a first-order loop filter. The delay line, consisting of cascaded variable delay stages, is driven by the input reference clock, *ckref*. The output of the delay line's final stage and the *ckref* falling edges are compared by the phase detector to determine the phase alignment error. The phase detector output is integrated by the charge pump and loop filter capacitor to generate the control voltage, *vcntl*, of the delay stages.

When correctly locked, the total delay of the delay line should equal one period of the reference clock. A conventional

Manuscript received July 19, 2000; revised October 24, 2000. This work was supported by Parthus Technologies.

D. J. Foley is with the Department of Microelectronics, National University of Ireland, Cork, Ireland.

M. P. Flynn is with Parthus Technologies, Cork, Ireland.

Publisher Item Identifier S 0018-9200(01)01483-4.

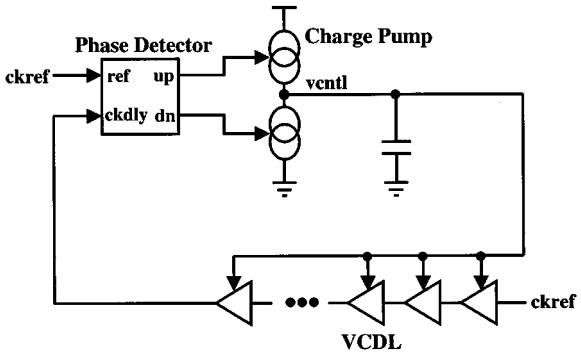


Fig. 1. Conventional DLL architecture.

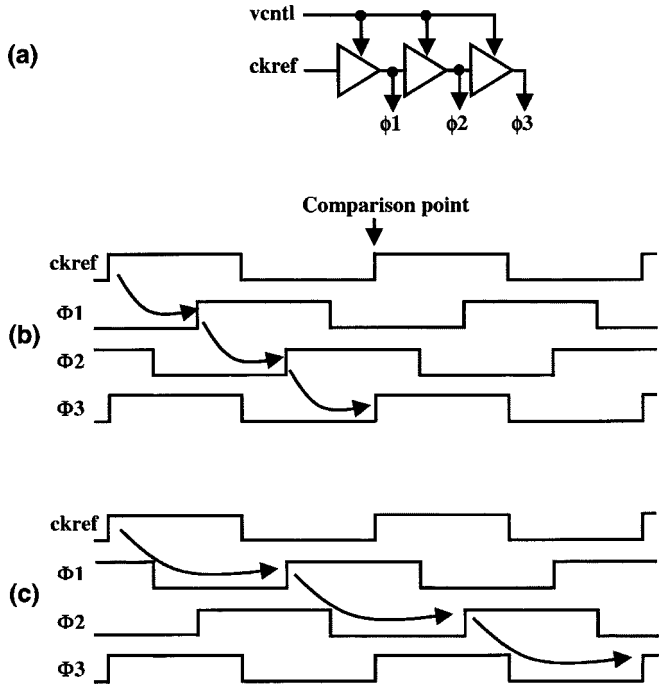


Fig. 2. (a) Three-stage VCDL. (b) Waveforms with correct lock. (c) Waveforms with false lock.

DLL may lock or attempt to lock to an incorrect delay. In Fig. 2 we show correct and false locking for a three-stage delay line [Fig. 2(a)]. Fig. 2(b) shows the output phases at each stage ($\phi 1, \phi 2$, and $\phi 3$) with the delay line in correct lock. The DLL control loop has aligned $\phi 3$ and *ckref*. The total delay is one period of the reference clock. In Fig. 2(c) $\phi 3$ and *ckref* are again aligned but the total delay is two clock periods. The DLL can also falsely lock to three or more periods of delay or can attempt to lock to zero delay.

B. Self-Correcting DLL Architecture

Fig. 3 shows a block diagram of the new self-correcting DLL. The problem of false locking is solved by the addition of a lock-detect circuit and by some slight modifications to the conventional phase detector. The DLL incorporated in the two designs reported in this paper employs a nine-stage VCDL as shown in Fig. 3.

In a conventional DLL, only the state of the output of the last delay element is used. From the example in Fig. 2, we can see that the state at the outputs of the other delay elements can

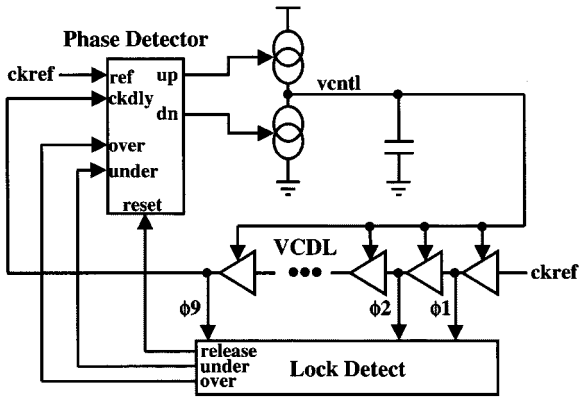


Fig. 3. Self-correcting DLL architecture.

provide additional information about the nature of the locked delay. In the prototype the delayed phases, ϕ(1:9), are decoded to indicate the VCDL delay. If the delay is outside an acceptable delay range then the lock-detect circuit takes control of the loop from the phase detector. The lock-detect circuit signals the charge pump to charge or discharge the filter capacitor until it is safe for the phase detector to regain control of the loop.

Three control signals are produced by the lock-detect circuit: *over* to indicate that the VCDL delay is greater than 1.5 reference clock periods, *under* to indicate that the delay is less than 0.75 clock periods, and *release* is activated when the delay reaches 1.25 clock periods. The *release* signal clears the *over* and *under* control signals and removes the phase detector from reset. The phase detector then regains control of the loop. If neither *under* nor *over* is active then the phase detector has control of the loop and the DLL is either in correct lock or approaching correct lock.

If the DLL is in lock and it is brought out of lock because of missing reference clock pulses or a step in the input reference frequency, then the DLL may inadvertently try to lock to an incorrect delay. The DLL is allowed to attempt to reach the undesired lock delay until it triggers either an *over* or an *under* signal at which time the lock-detect circuit takes control of the DLL loop.

C. Lock-Detect Circuit

The VCDL output phases are first level shifted to CMOS levels. The level shift circuitry is designed to have high gain and fast rise and fall times. This helps to minimize any jitter contribution from this circuitry. The level-shifted output phases, ϕ(1:9), are latched on the rising edge of the reference clock. The outputs from these latches are processed by the decode circuitry as shown in the schematic of Fig. 4. The inputs, Q(1:8), correspond to the ϕ(1:8) output phases of the VCDL. Fig. 5 shows example output waveforms for a nine-stage VCDL. In Fig. 5(a) when the state of the VCDL output phases is decoded none of the control signals are activated as the VCDL is correctly locked to one period of the reference clock. In Fig. 5(b) the VCDL is incorrectly locked to two periods of the reference clock and the state of the output phases is decoded to activate the *over* control signal.

The phase detector outputs, *up* and *dn*, signal the charge pump to charge or discharge the filter capacitor. An active *over* output

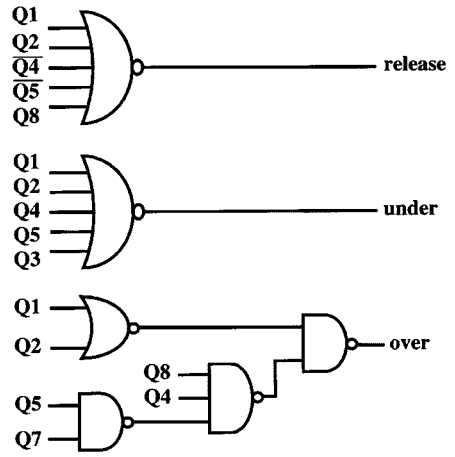
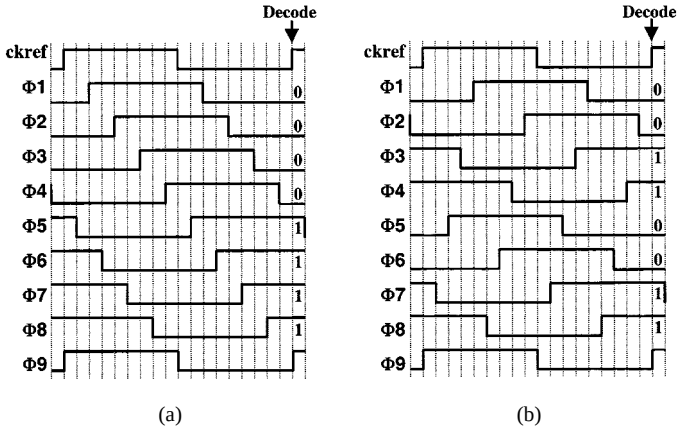


Fig. 4. Lock-detect decode circuitry.



(a) (b)

Fig. 5. Nine-stage VCDL waveforms with (a) correct lock and (b) false lock.

from the lock-detect circuit disables the phase detector and activates the *up* control signal. Similarly, the lock detect *under* output activates *dn*. Following power-on reset the lock-detect circuit is initialized by setting *over* active. This ensures a faster acquisition time for the DLL because the filter capacitor is continuously charged to a voltage level corresponding to 1.25 reference clock periods. At this VCDL delay, the *release* signal is activated and the phase detector gains control of the loop and brings the DLL to lock. The state of the output phases corresponding to a delay of nine reference clock periods is the same as that corresponding to a single reference clock period delay. This circuitry is therefore only capable of detecting incorrect delays up to eight periods of the reference clock. This is not a limitation of the design as any delays above this would be outside the delay range of the VCDL. In general, the error detection logic can detect an incorrect lock delay up to $N-1$ periods of the reference clock, where N is equal to the number of VCDL output phases.

D. Voltage-Controlled Delay Line (VCDL)

Fig. 6 shows one of the VCDL delay stages. The stage is designed to operate from a supply as low as 1.8 V and is similar to that used in [7]. The stage propagation delay is proportional to the tail current for the output charging and to the voltage-controlled resistor (VCR) resistance for the output discharging.

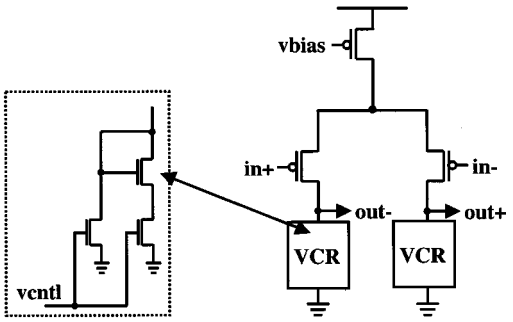


Fig. 6. VCDL delay stage schematic.

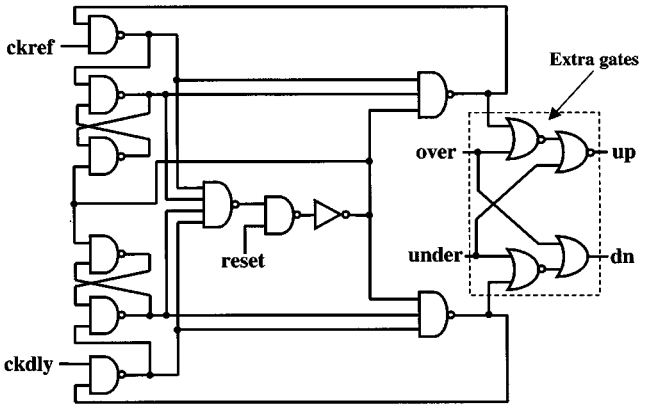


Fig. 7. Phase detector schematic.

A three-transistor VCR structure is adopted for better control linearity. The DLL negative feedback control loop compensates for variations in the stage delay due to process and temperature. The differential delay stage structure and coupling capacitors between bias lines and supply help to minimize supply-induced jitter noise.

E. Charge Pump

The charge pump charges or discharges the filter capacitor. The voltage on this capacitor, *vcntl*, sets the VCDL stage propagation delay. To minimize the temperature variation of the VCDL delay, the charging and discharging currents are proportional to absolute temperature. This helps to maintain a constant loop gain and phase margin over temperature.

F. Phase Detector

The phase detector, shown in Fig. 7, employs the conventional sequential-phase-frequency detection scheme [7] but extra gates have been included. This extra logic enables the lock-detect circuit to over-ride the phase detector control of the loop. The lock-detect output signals, *over* and *under*, now have direct control of the charge pump. The lock-detect circuit can therefore charge or discharge the VCDL control voltage, *vcntl*, to a voltage from which it is safe for the phase detector to regain control of the loop.

III. Clock Synthesizer Architecture

The clock synthesizer generates a differential output clock running at nine times the input reference frequency. The clock

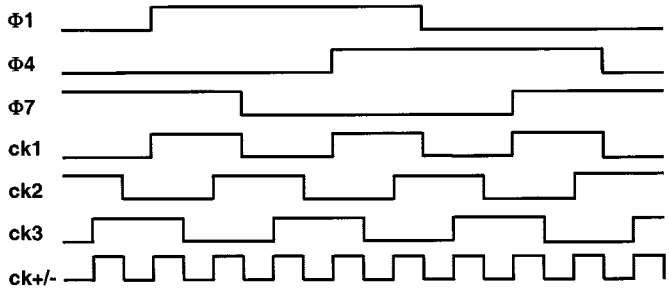


Fig. 8. Clock synthesis waveforms.

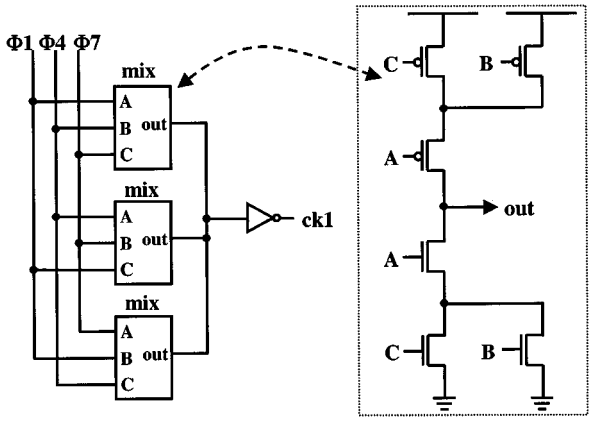


Fig. 9. Optimized AND-OR block diagram.

synthesizer employs the DLL structure shown in Fig. 3 to generate the multiple clock phases that are then combined to produce the output clock. There are two steps in the generation of the output clock. The first step combines the nine DLL output phases, $\phi(1{:}9)$, to generate three clocks ck1, ck2, and ck3. Fig. 8 shows the clock waveforms. These three clocks are phase separated by one-ninth of a reference clock period and have a frequency three times that of the reference clock. Fig. 9 shows how the $\phi 1$, $\phi 4$, and $\phi 7$ output phases are combined in an optimized AND-OR structure with symmetrical delays to generate the ck1 clock. Using identical logic the $\phi 2$, $\phi 5$, and $\phi 8$ phases produce the ck2 clock and the $\phi 3$, $\phi 6$, and $\phi 9$ phases produce the ck3 clock.

The second step in generating the synthesizer output clock is to combine these three clocks in another AND-OR structure to produce a differential output clock, $ck+$ and $ck-$, running at nine times the reference clock frequency; see Fig. 8. This design produces a 1.62-GHz output clock frequency for a 180-MHz reference clock frequency. For a 0.5-μm 3.3-V CMOS process there is a bandwidth limitation of approximately 500 MHz for reliable on-chip clock transmission [8]. The high bandwidth available at the chip outputs is utilized (determined by the external pull-up resistor and load capacitance) [8] to produce the 1.62-GHz clock as shown in Fig. 10. The AND function of the clock generation is performed in the chip core and the analog OR function is performed in the I/O ring. External pull-up resistors set the output swing and match the output impedance to that of the test equipment. Damping resistors are included to avoid any oscillations resulting from the combination of the lead and pin inductance and load capacitance. This removes the necessity to double bond these high-frequency outputs.

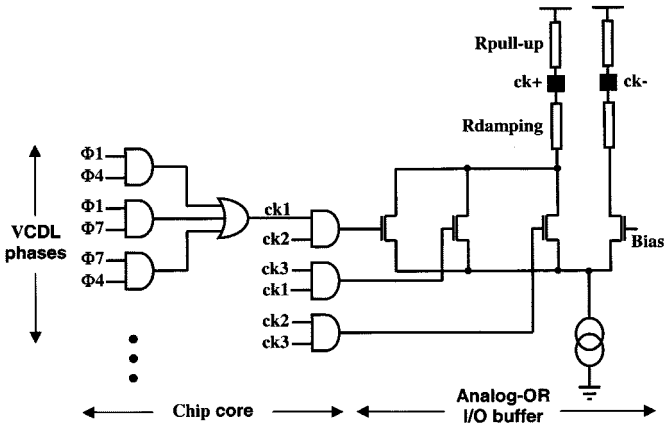


Fig. 10. 1.62-GHz clock generation schematic.

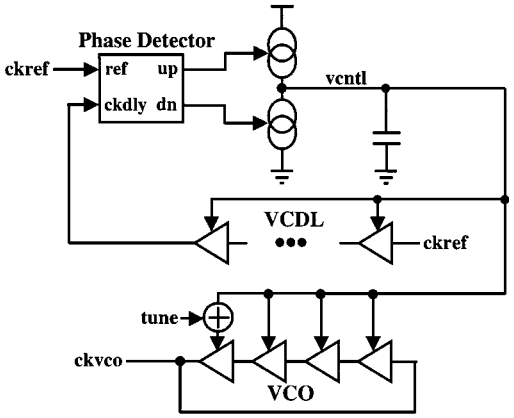


Fig. 11. Tunable VCO architecture.

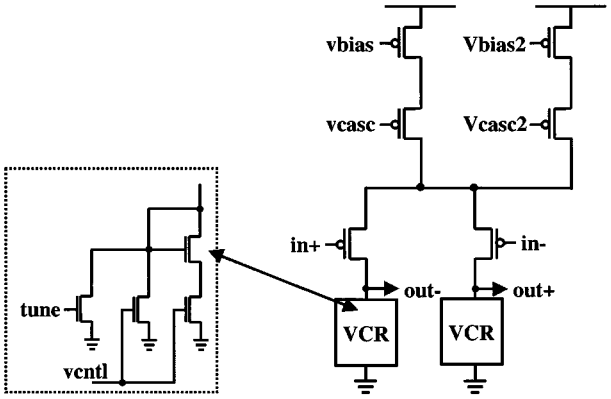


Fig. 12. Tunable VCO stage block diagram.

IV. Temperature-Compensated Tunable VCO Architecture

The temperature-compensated oscillator utilizes the control loop voltage, *vcntl*, of the DLL (Fig. 3) to compensate for any temperature and supply voltage induced frequency fluctuation in a VCO. Fig. 11 shows how the VCO and VCDL stages are both connected to *vcntl*. (For ease of illustration a conventional DLL is shown in Fig. 11 but in practice the new DLL architecture of Fig. 3 is employed). The VCDL in the DLL tracks temperature and process variations in the VCO circuit. The VCO is

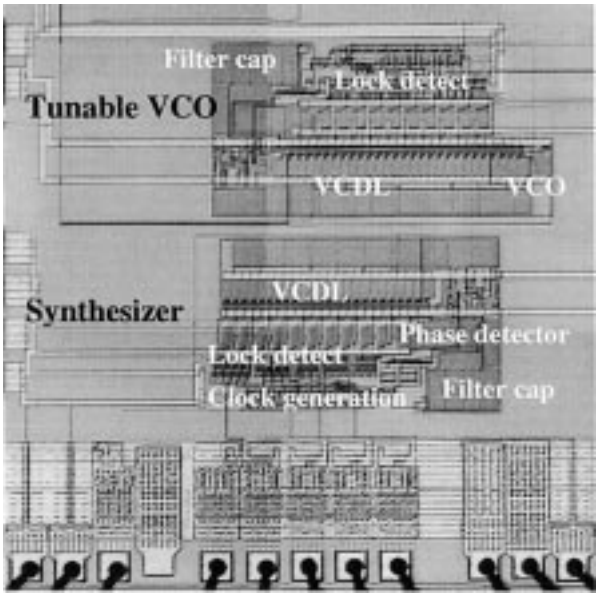


Fig. 13. Die photo of the synthesizer and tunable oscillator.

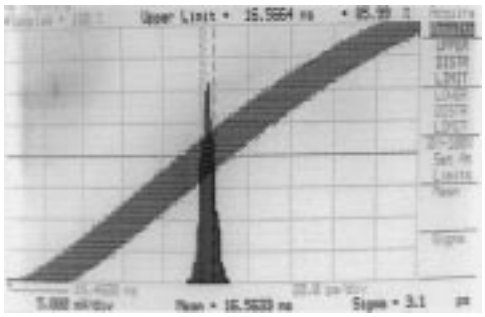


Fig. 14. 1.62-GHz synthesizer edge jitter histogram.

composed of the same delay stages as the VCDL and its temperature (and process) variations will therefore be the same (apart from some minor random mismatch effects and thermal gradients across the die). *vcntl* thus compensates for the VCDL and VCO temperature fluctuations. The last VCO stage has an additional tuning voltage, *tune*, which fine tunes the VCO frequency. By varying the tune voltage it is possible to tune the VCO center frequency to within $\pm 3\%$. A wider tuning range can be achieved by varying the frequency of the DLL reference clock, *ckref*.

The schematic of the last VCO stage is shown in Fig. 12. This stage is identical to the other VCO and VCDL stages except that the VCR contains a transistor which is connected to the external *tune* voltage. In all other stages this transistor is connected to ground. The extra charging current required in this VCO stage is provided by the controlled current source bias V_{bias2}.

V. Circuit Layout

The synthesizer and temperature-compensated tunable oscillator were fabricated on a standard 0.5-μm triple-metal single-poly digital CMOS process. The die photomicrograph of the device, containing both the synthesizer and temperature-compensated tunable oscillator, is shown in Fig. 13. The synthesizer has an active area of 0.6 mm^2 and the temperature-compensated tunable oscillator has an active area of 0.7 mm^2.

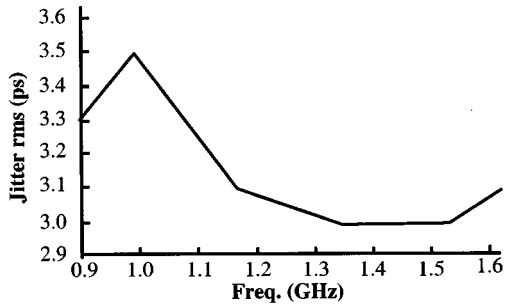


Fig. 15. Variation of measured jitter over output frequency.

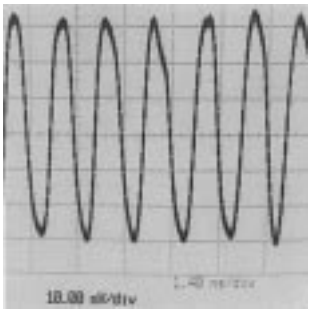


Fig. 16. 720-MHz synthesizer output for $V_{\text{DD}} = 1.8$ V.

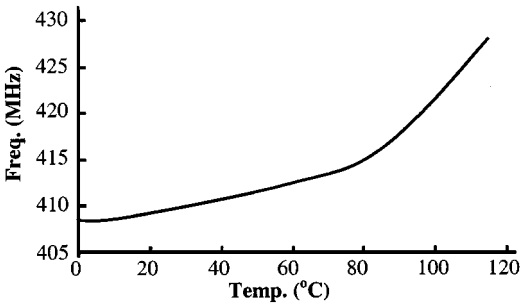


Fig. 17. VCO frequency variation with temperature.

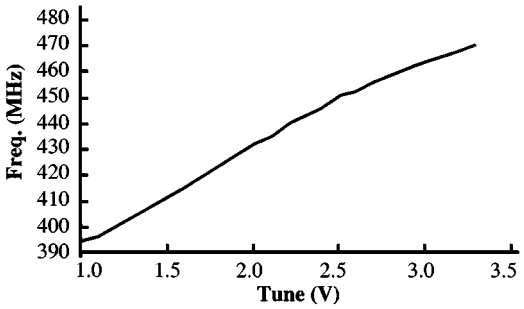


Fig. 18. VCO frequency variation with tune voltage.

VI. Test Results

Fig. 14 shows a histogram of the edge jitter on the 1.62-GHz synthesizer output clock for a supply of 3.3 V. Edge jitter of 3.1 ps rms and 20 ps peak-to-peak were measured. The jitter measurements of 3.2 ps rms and 20 ps peak-to-peak, for a 2-V supply and 1-GHz output frequency, show that the DLL core ex-

TABLE I
MEASURED SYNTHESIZER CHARACTERISTICS

1GHz Edge jitter (peak-to-peak)	< 20ps
1GHz Edge jitter (rms)	3.2ps
1GHz inter-period jitter	100ps
Power supply	1.8-3.3V
Current consumption @ 2V:	
Synthesizer	20mA
Output Driver	7mA
Output Clock Frequency Range @ 2V	600MHz to 1GHz
Output Clock Frequency Range @ 3.3V	900MHz to 1.6GHz
On chip loop filter capacitor	20pF
Loop Bandwidth	1MHz
Active area	0.6mm^2
Process	0.5μm CMOS
Device package	44-pin CLCC
PCB substrate	FR4

TABLE II
MEASURED TUNABLE OSCILLATOR CHARACTERISTICS

400MHz frequency variation over temperature range 0 to 85°C	1.8%
Frequency Tuning Range	200MHz to 500MHz
400MHz Edge Jitter (rms)	29ps
400MHz Edge Jitter (peak-to-peak)	180ps
VCO supply sensitivity (open loop)	0.83%/V
Power supply	3.3V
Current Consumption @ 3.3V:	
DLL + Tunable VCO	42mA
Output Driver	6mA
Active area	0.7mm^2
Process	0.5μm CMOS

hibits better jitter performance than that reported for the higher voltage DLLs (3.3-V supply, 0.35-μm CMOS, 4-ps rms jitter) in [2] and (5-V supply, 0.7-μm CMOS, 10-ps rms jitter) in [3]. The measured jitter (rms) variation versus synthesizer output frequency for a 3.3-V supply is shown in Fig. 15. With the supply reduced to 1.8 V, the rms jitter was measured at 4.9 ps for an output frequency of 720 MHz. Fig. 16 shows this 720-MHz synthesizer output. Mismatched propagation delays and interblock routing in the frequency multiplication block (Fig. 9) resulted in 100-ps interperiod jitter.

Fig. 17 shows the temperature-compensated tunable oscillator frequency variation with temperature. Varying the ambient temperature from 0 °C to 85 °C resulted in a total frequency variation of 1.8%. Fig. 18 shows the variation of frequency with the tune voltage. As can be seen from the plot, the relationship is close to linear. It is possible to tune the frequency around a center frequency in the range from 200 to 500 MHz by selecting an appropriate input reference frequency. This ensures that this scheme can be used for a wide variety of applications. The measured jitter on the 400-MHz output was 29 ps rms and 180 ps peak-to-peak. Table I shows the measured synthesizer characteristics. Table II summarizes the measured characteristics of the temperature-compensated tunable oscillator.

VII. CONCLUSION

In this paper, a robust self-correcting low-jitter DLL was used as the basis for a low-voltage high-frequency synthesizer and a temperature-compensated tunable oscillator. The DLL does not require the VCDL control voltage to be set on power-up. The DLL can recover from missing reference clock pulses and it can track step changes in a variable reference clock frequency. The synthesizer has significantly lower edge jitter than the traditional PLL-type synthesizer [9] and other reported DLL circuits [10], [11]. The temperature-compensated tunable oscillator provides a temperature-stable tunable frequency that varies by just 1.8% over the 0 °C to 85 °C temperature range.

ACKNOWLEDGMENT

The authors wish to acknowledge contributions from the following Parthus Technologies employees: J. Ryan, J. Horan, C. Cahill, F. Fuster, J. Collins, B. Kinsella, M. Erett, and S. Murphy. The authors also wish to thank R. Fitzgerald from the NMRC for the die photo micrographs. The device was fabricated on the ESM (Newport) Wafer Fab through Europractice.

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David J. Foley (S'00) received the B.Eng. degree from the National University of Ireland, Limerick, in June 1988. In 1994 he received the M.Eng.Sc. degree from the National University of Ireland, Cork, where he is currently working toward the Ph.D. degree.

He has worked in IC design with NEC Corporation, Tamagawa, Japan, from 1988 to 1990, AT&T Bell Labs, Tokyo, Japan, from 1990 to 1992, and Parthus Technologies, Dublin, Ireland, from 1994 to 1998.

Michael P. Flynn (S'92–M'95–SM'98) was born in Cork, Ireland. He received the B.E. and M.Eng.Sc. degrees from the National University of Ireland, Cork, in 1988 and 1990, respectively. He received the Ph.D. degree in electrical engineering from Carnegie Mellon University, Pittsburg, PA, in 1995.

From 1998 to 1991, he was with the National Microelectronics Research Center, Cork. He was a Co-op Engineer with National Semiconductor in Santa Clara, CA, from 1993 to 1995. From 1995 to 1997, he was a Member of Technical Staff with Texas Instruments DSPS R&D Lab, Dallas, TX. He is now a Technical Director with Parthus Technologies, Cork. He is also a part-time Lecturer in the Department of Microelectronics at the National University of Ireland, Cork.

Dr. Flynn received the 1992–1993 IEEE Solid-State Circuit Predoctoral Fellowship. He is a member of Sigma Xi.