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A 3.3V, 1.6GHz, Low-Jitter, Self-Correcting DLL Based Clock Synthesizer in 0.5μm CMOS.

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ABSTRACT

This paper describes a 1.6GHz clock synthesizer which employs a delay locked loop (DLL) to generate multiple phases that are combined to produce the desired output clock frequency. A self correcting circuit ensures that the DLL arrives at the correct locked state irrespective of its power-up state or following either a wide variation in the input reference clock frequency or missing pulses in this clock signal. The measured edge peak-to-peak and rms jitter for a 1.6GHz output clock was 20ps and 3.1ps respectively. The circuit is powered from a 3.3V supply and was fabricated on a 0.5μm generic digital CMOS process.

I. INTRODUCTION

Many applications including communication circuits require clock or edge synthesis. Traditionally phase locked loops (PLL) have been used. In a PLL the voltage controlled oscillator (VCO), when combined with a divider in the feedback path, can run at desired multiples of the reference frequency [1], [2]. The synthesizer outlined in this paper employs a DLL. A DLL provides greater stability than higher order PLL's and requires only one capacitor in its first order loop filter. This capacitor can usually be incorporated in the chip core. A PLL on the other hand generally requires a more complex second order filter. This filter usually employs larger components which may need to be off chip. Additionally, a DLL offers better jitter performance than a PLL because phase errors induced by supply or substrate noise do not accumulate over many clock cycles [3].

To function correctly a DLL should lock to a single period of the reference clock. However a DLL may falsely lock onto a multiple of this period. A conventional DLL may also attempt lock to zero delay. Figure 1 illustrates a false locking scenario for a DLL employing a nine stage voltage control delay line (VCDL) similar to that used in this paper's synthesizer. The first set of waveforms show a DLL correctly locked to one period of the reference clock. The DLL aligns the ckref and VCDL output, $\phi 9$, falling edges. In the second set of waveforms the ckref and $\phi 9$ falling edges are again aligned, however, the DLL is in this case locked to two ckref periods of delay. To avoid this problem the DLL's voltage control delay line (VCDL) control voltage has been traditionally set to a particular voltage on power-up and the VCDL has a restricted delay range. This works if there is tight control of the control voltage to VCDL delay and if the DLL is not required to lock onto a variable input reference frequency. Additionally, if the reference clock to the DLL has some missing pulses, due perhaps to a system interrupt, the DLL can try to lock to an incorrect delay after the reference clock returns to normal.

A self-correcting DLL scheme introduced in this paper overcomes these problems. A synthesizer employing this DLL proves that the scheme works successfully over a wide range of reference clock frequency. The self-correcting circuit detects when the DLL is locked, or is attempting to lock, to an incorrect delay and can then bring the DLL back into a correct locked-state. The DLL no longer requires the VCDL control voltage to be set on power-up, it can recover from missing reference clock pulses and it can accommodate a variable reference clock frequency.

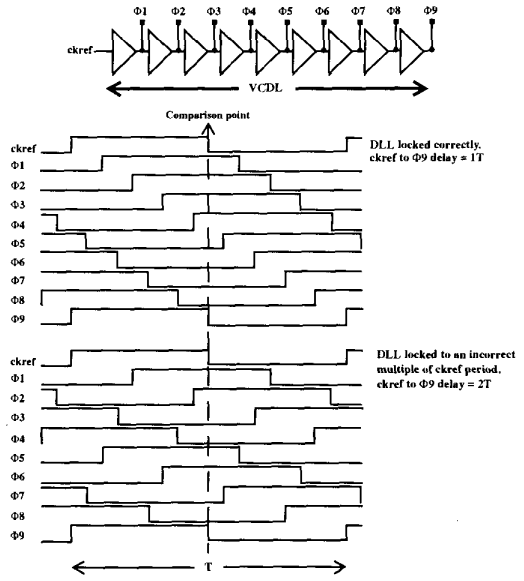

FIGURE 1. VCDL output clock phase waveforms for a DLL locked to two different delays.

II. ARCHITECTURE

A simplified block diagram of the synthesizer is outlined in Figure 2. This circuit comprises of a voltage controlled delay line (VCDL), a phase detector (PD), a charge pump, a first order loop filter capacitor, a clock generation circuit and a lock detect circuit. The VCDL, consisting of cascaded variable delay stages, is driven by the reference input clock, ckref. The VCDL final stage output, $\phi 9$, and the ckref falling edges are compared by the PD to determine the phase alignment error. The PD output is integrated by the charge pump and

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loop filter capacitor to generate the delay stages control voltage, vcntl. The VCDL output clock phases, $\phi(1:9)$, are processed by the lock detect circuit to determine if the DLL is locked or is attempting to lock to an incorrect delay. If an error is detected the lock detect removes the PD from the control loop and signals the charge pump to charge or discharge the filter cap to a voltage level from where it is safe to return control of the loop to the PD. Clock phases, $\phi(1:9)$, are combined together in the clock generator circuit to produce the frequency multiplied output clock, nck4. A level shift circuit converts the differential outputs of the VCDL stages to CMOS levels.

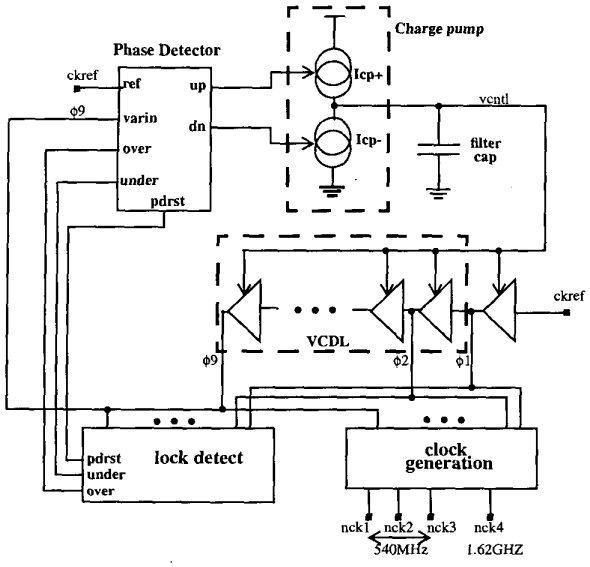

FIGURE 2. Clock synthesizer block diagram.

III. CIRCUIT DESIGN

A. Lock Detect.

The VCDL output phases, $\phi(1:9)$, are latched by the lock detect circuit. The state of these phases is decoded to indicate the VCDL delay. Three control signals are produced: "over" to indicate that the VCDL delay is greater than 1.5 reference clock periods, "under" to indicate that the delay is less than 0.75 clock periods and "pdrst" is activated to reset the phase detect circuit when the VCDL delay has reached 1.25 clock periods. Consider for example the case where the DLL is attempting to lock to zero delay. The $\phi(1:9)$ outputs would all be equal to zero and this would result in the "under" signal being generated. In Figure 1 it is also possible to see that in the first set of waveforms the state of the $\phi(1:9)$ outputs are different at the comparison point than their state in the second set of waveforms. Their state in the second set of waveforms would be decoded in the lock detect circuit to set the "over" control signal. The VCDL delay range is sufficient to trigger these control signals over all process, voltage, and temperature combinations. If none of the three control signals is active then the phase detect has control of the loop and the DLL is either in lock or approaching lock. If the DLL is in lock and it is brought out of lock by some missing reference clock pulses or a step in the input reference frequency then the DLL can inadvertently try to lock to an incorrect delay. The DLL is allowed to attempt to reach the undesired lock delay until it triggers either an "over" or an "under" signal. Then as explained above the lock detect circuit takes control of the DLL loop. The circuit used to decode the nine stage VCDL outputs is capable of detecting incorrect delays up to 8 periods of the reference clock. This is not a limitation for the design as any delays above this would be below the range of the VCDL. It follows that this error detection logic can detect an incorrect lock delay up to N-1 periods of the reference clock, where N is equal to the number of VCDL output phases.

B. Voltage controlled delay line (VCDL).

Figure 3 illustrates one of the VCDL delay stages [1]. The stage propagation delay is proportional to the tail current for the output charging and to the voltage controlled resistor, VCR, resistance for the output discharging. The VCR control voltage to current sink linear range is maximised to improve the linear range of the stages's control voltage to propagation delay. The DLL control loop compensates for variations in the stage delay due to process and temperature. Supply induced jitter noise is minimized by using a differential structure with a cascoded current source.

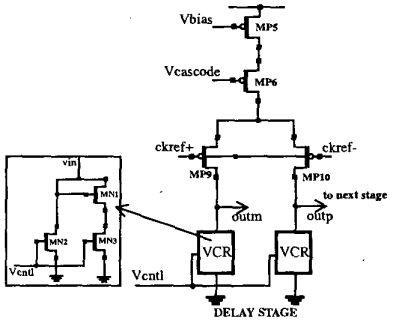

FIGURE 3. VCDL delay stage biasing schematic.

C. Charge Pump.

The charge pump charges/discharges the filter capacitor and the voltage on this capacitor, vcntl, sets the delay stage propagation delay. To minimize the temperature variation of the VCDL delay the charging and discharging currents are proportional to absolute temperature.

D. Filter capacitor.

An N-channel MOSFET gate capacitance is used to provide the 25pF filter capacitance. Careful layout ensures optimum channel and adjacent transistor interconnect resistance.

E. Phase detector (PD).

The phase detector, PD, shown in Figure 4, employs the conventional sequential frequency and phase detection circuit [1] but has the extra gates NR2-1, NR2-2, NR2-3, OR2-1, IV4 and IV5. These extra gates have been added to enable the lock detect circuit to override the PD control of the loop. This results in the lock detect circuit setting the "under" or "over" signals to charge or discharge the VCDL control voltage, vcntl, and hence the loop does not lock to an incorrect delay. The lock detect relinquishes control of the loop when it detects that vcntl has reached a level such that the VCDL delay is just over one reference clock period. The PD is then reset so that it starts in a correct state.

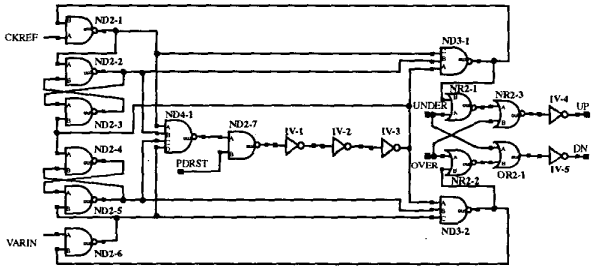

FIGURE 4. Phase detector schematic.

F. Clock Generator.

To generate the output clock the VCDL output phases, $\phi(1:9)$, are first combined in an optimized AND-OR structure with symmetrical propagation delays. Figure 5 illustrates the combination of the $\phi 1$, $\phi 4$ & $\phi 7$ phases to generate the nck1 clock (which runs at three times the input reference clock frequency). The clock waveforms are shown in Figure 6. The $\phi 2$, $\phi 5$ & $\phi 8$ phases produce the nck2 clock and the $\phi 3$, $\phi 6$ & $\phi 9$ phases produce the nck3 clock. These three clocks, nck1, nck2 & nck3 are phase shifted by one ninth of the reference clock frequency (Figure 6). These clocks are then combined in an AND-OR structure to produce an output clock, nck4, having nine times the reference clock frequency. This design produces a 1.62GHz output clock frequency for a 180MHz reference clock frequency. For a 0.5µm, 3.3V, CMOS process there is reliable bandwidth limitation for on-chip clock transmission of approximately 500MHz [4]. The high bandwidth available at the chip outputs is therefore utilised (determined by the external pull-up resistor and load capacitance). The 1.62GHz clock is produced at the chip output as shown in Figure 7. The AND function of the clock generation is performed in the chip core and the analog OR function is performed in the I/O buffer area. External load resistors set the output swing and match the output impedance to that of the test equipment

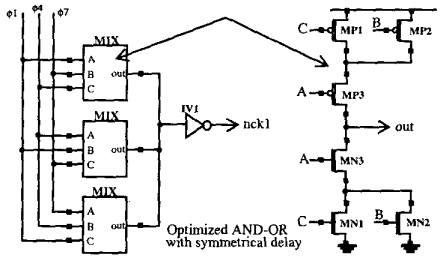

FIGURE 5. Clock frequency multiply X3 circuit.

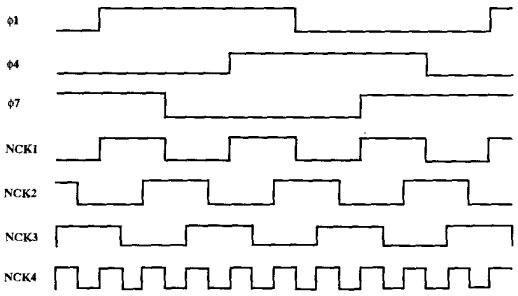

FIGURE 6. Clock generation waveforms.

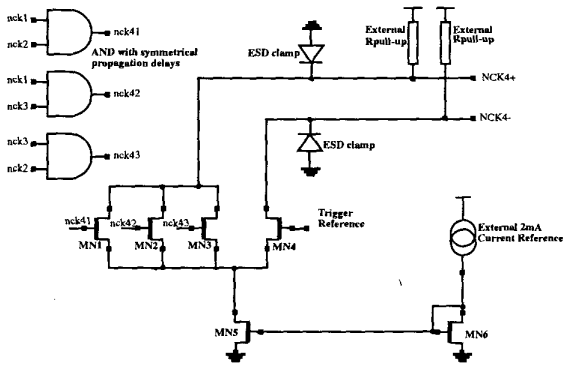

FIGURE 7. 1.62GHz clock generation schematic.

G. Chip layout.

The chip was fabricated on a standard 0.5µm, triple metal, single poly, digital CMOS process. The layout of the DLL synthesizer is shown in Figure 8. The active die area is 0.6mm^2.

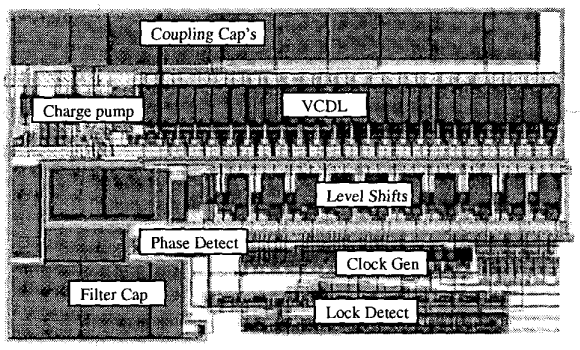

FIGURE 8. DLL synthesizer layout.

IV. TEST RESULTS

Figure 9 shows a histogram of the edge jitter on the 1.62GHz output clock. RMS edge jitter of 3.1ps and peak-to-peak edge jitter of 20ps were measured. Similar results were obtained for various output clock frequencies between 900MHz and 1.62GHz. 100ps inter-period jitter was measured on the 1.62GHz output clock. This inter-period jitter was caused by mismatched propagation delays between the clock phases driving the clock generation block. It can be greatly reduced by improving the inter-block routing. Table 1 outlines the DLL synthesizer characteristics.

TABLE I-Measured Synthesizer Characteristics.

1.62GHz Edge jitter (pk-pk)	20ps
1.62GHz Edge jitter (RMS)	3.1ps
1.62GHz inter-period jitter	100ps
Power supply	3.3V
Current consumption:	
Synthesizer	40mA
Output Driver	10mA
Output Clock frequency range	0.9-1.62 GHz
Active area	0.6mm^2
Process	0.5μm CMOS

V. SUMMARY

This paper describes a 1.62GHz CMOS clock synthesizer with significantly lower edge jitter than the traditional PLL type synthesizer. [2] and reported DLL circuits [5], [6], [7]. The self-correcting circuit incorporated in the synthesizer results in a more robust DLL. The DLL no longer requires the VCDL control voltage to be set on power-up. The DLL can recover from missing reference clock pulses and it can track step changes in a variable reference clock frequency.

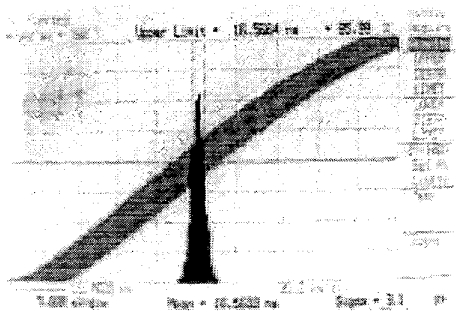

FIGURE 9. Measured 1.62GHz output clock edge jitter.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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