A BiCMOS Preamplifier/Write-driver IC for Tape Drive

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Abstract - A single-supply 5V preamplifier IC for magneto-resistive (MR) read element tape drive is described. The IC incorporates six independent read amplifiers, and four independent write drivers. The read amplifier is a fully differential current sense circuit. MR bias current direction steering is incorporated without additional switches in the signal path. In addition the IC incorporates a voltage reference, head diagnostics, control registers, and a serial interface. The entire IC, built in a 1.2μm BiCMOS process, occupies 36mm^2. With a 39 Ohm read element the measured input referred noise is 1.0nV/$\sqrt{}$Hz.

I. Introduction

Magneto-resistive (MR) elements are now used to sense recorded data in hard disk and tape drive systems. A preamplifier IC provides a bias current for the MR element and amplifies the small signal detected by the element. In a HDD system, data is read or written to a single head; in a tape drive system a number of tracks may be read or written concurrently. Compared to hard disk drive the data rate in a tape system tends to be lower, however the lower operating frequency necessitates better low frequency noise performance. Because of environmental noise, and because tape preamp connects with a flex cable to the read/write head, a fully differential solution is required. For cost reasons the preamp should require only a single 5V supply.

A MR element typically requires a bias current of between 5mA and 15mA. An additional requirement in tape systems is that the head current direction can be reversed. Current direction switching adds further complexity and may increase noise. In disk and tape systems, to prevent arcing with the case or head shield, it is often necessary either to fix or to determine the mid-point voltage of the head.

There are two categories of preamp, usually called *current sensing*, and *voltage sensing*. In voltage sensing the small signal voltage across the MR element is amplified. In current sensing the amplifier presents a low impedance, and the small signal changes in current are amplified. The current sensing technique has some advantages. Current sensing tends to compensate for resistance changes in the MR element [1]. Because of the low input impedance, the read bandwidth is less effected by parasitic capacitance. Current sensing also offers the possibility of reusing some of the MR element current in the amplifier bias.

A bipolar differential current sense scheme is described in [1] but it requires dual supplies. Another differential current sensing scheme is described in [2] (and also later in [3]). A 5V CMOS preamp IC for tape drive, with 4 single ended current sense read amplifiers, and without write drivers was presented [4]. The single supply 5V preamp IC described in this paper, implements a differential current sense amplifier (six independent channels), that incorporates low noise MOS current sources and current direction switching. Four independent write channels, diagnostics and control logic are also included on the IC.

II. Read Amplifier

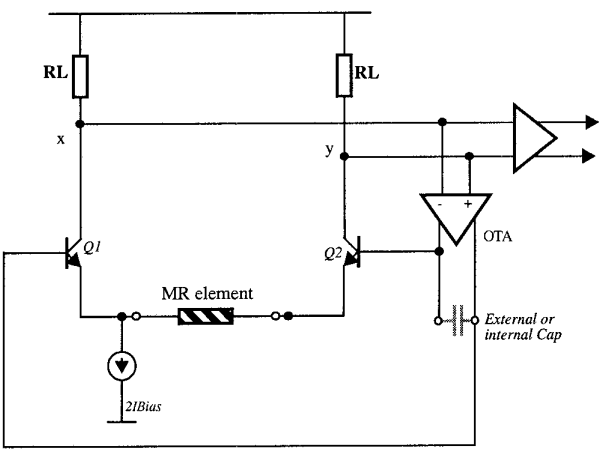

Fig. 1. Fully differential current bias, current sense front end, with single supply.

Fig. 1 shows a simplified current sensing front end similar to [3]. At low frequencies the feedback loop forces nodes x and y to be at the same potential. This causes the bias current to split equally between the two sense bipolars Q1 and Q2. The capacitor limits the bandwidth of the feedback loop. Above the feedback loop cutoff frequency, an amplified version of the AC head voltage appears across the load resistor RL at nodes x and y. Additional gain is provided by a second stage amplifier.

Fig. 2 shows a modified version of the front end. A second current source (IMRBTop) connects to the MR element. The MR current is programmable, the reduced fixed current flows through Q1 and Q2, and the programmable part is supplied by IMRBTop. Cascode devices isolate the gain nodes from the large collector parasitic capacitances of Q1 and Q2. Addi-

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tional bias is injected at the cascode nodes, further reducing the quiescent current at the load resistors, allowing larger resistors to be used.

The OTA is fully differential and includes common mode feedback. This feedback fixes the common mode of the base voltages of Q1 and Q2, and thus also the mid point voltage of the MR element. In this way no extra devices are connected to the sensitive MR head. The on-chip capacitors C2 and C3 compensate the common mode feedback loop.

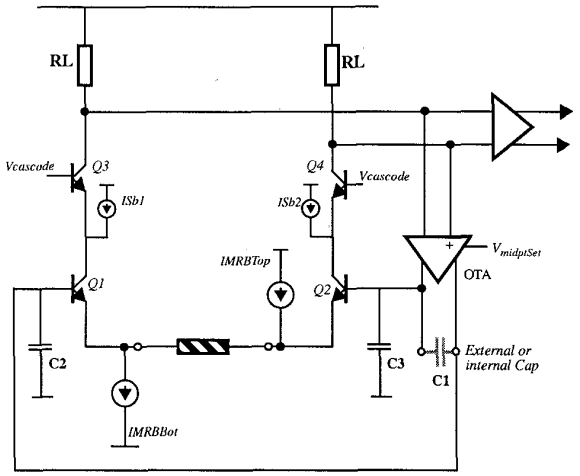

Fig. 2. Fully differential current bias, current sense front end, with single supply.

Current bias direction switching could be implemented by introducing multiplexor switches at the connection to the MR element. However such switches would add thermal noise and might also couple environmental noise onto the preamp signal. A HBridge type solution was adopted (see Fig. 3). In the figure two top current sources (*IMRBTopL* and *IMRBTopR*) and two bottom current sources (*IMRBBotL* and *IMRBBotR*) are connected to the MR element. Only one top and one bottom source from opposite sides supply current. The head bias can flow in either direction, there are no switches in the signal path or in the feedback loop.

In tape or disk systems it is often useful to monitor the resistance of the MR element to detect aging or failure. This can be difficult in voltage sense schemes, especially so when the MR element is capacitively coupled to the amplifier input. In addition, extra circuitry connected to the MR element will add noise and may introduce crosstalk.

In this implementation the MR resistance is derived from the difference in base voltages of Q1 and Q2. This difference voltage is a filtered version of the voltage across the MR head. In this way the MR resistance can be monitored (even during read) without introducing noise.

The gain of the first stage is set by the ratio of the load resistance and the total resistance at the input:

$$Gain = \frac{2R_L}{R_{MR} + 2r_e} \qquad \text{(EQ 1)}$$

where R_{MR} is the MR element resistance, RL is the first

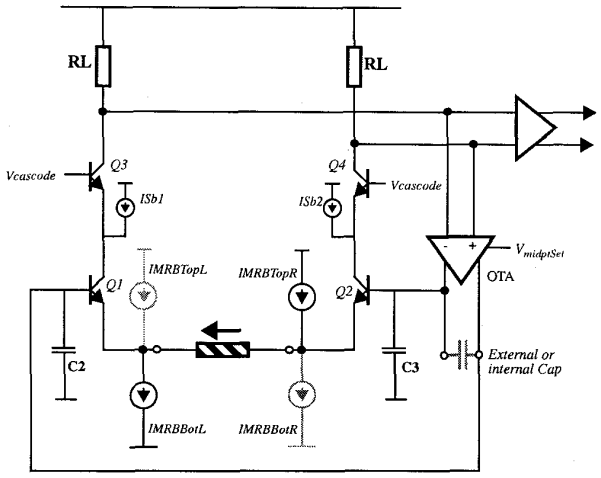

Fig. 3. Fully differential front end with current direction switching.

stage load resistor, and r_e is the emitter resistance of Q1 and Q2. The second stage provides additional variable gain of 10-20dB

As mentioned earlier, the OTA feedback loop has a limited bandwidth, this gives the first stage a high pass characteristic. The low frequency cutoff is given by:

$$w_{low} = \frac{2R_L}{R_{MR} + 2r_e} \frac{g_0}{2C_{diff}} \qquad \text{(EQ 2)}$$

where, g_0 is the transconductance of the OTA and C_{diff} is the effective capacitive load on the OTA (formed by C1,C2 and C3). In tape drive applications C_{diff} is large and therefore C3 is an external capacitor.

In a voltage sense amplifier, input bandwidth is dominated by capacitance, however in a current sense scheme the input bandwidth is dominated by the inductance at the input. Typically, in a tape drive a flex cable connects the MR element to the amplifier input. The pole at the input is given by Eqn. 3.

$$w_{p-input} = \frac{R_{MR} + 2r_e}{L_{input}} \qquad \text{(EQ 3)}$$

where L_{input} , the inductance at the input, is the sum of the flex cable and package inductance.

III. . Write Section

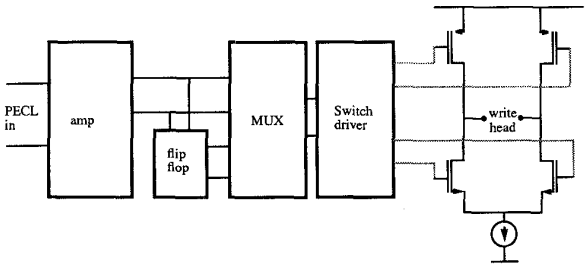

Fig. 4. Write driver circuitry

Fig. 4 shows the write driver. A simple CMOS HBridge supplies write current to the inductive load. A single current source shared by both NMOS bridge FETs determines the write current. Good pulse pairing is ensured by careful attention to matching and layout. An optional flip-flop can be included in the signal path to correct pulse pairing errors in the write data input.

IV. Full Chip

Fig. 5 is a block diagram of the entire IC. There are six independent read channels. Each read channel has an independently programmable MR bias, bias direction and gain. There are four independent write channels. Each has an independently programmable write current. The device can also measure head resistance and detect a number of faults including an open or shorted head. The analog functions and fault handling are controlled by a set of registers which are accessed through a four wire serial interface.

V. Experimental Results

The device was built with a 1.2μm BiCMOS triple-metal single-poly process. The die size, including pads, is 36mm^2. At 35MHz, with a 39 Ohm resistor at the input, the measured read amplifier input referred noise is 1.0nV/$\sqrt{Hz}$. (For comparison, with a 40 Ohm head, a single ended design [4] has a measured noise of 1.1nV/ $\sqrt{Hz}$ - Note, single ended circuits have fewer noise sources.) At 100KHz the measured input referred noise is 2.8nV/$\sqrt{Hz}$. Fig. 7 shows the variation of measured input-referred noise with frequency. These measurements were with a 5V supply and at room temperature. The read bandwidth is approximately 100MHz.

Fig. 6 shows the write driver current waveform with a 45mA write current and a 300nH load. The rise time is 3.4ns. With a 125nH load the rise time drops to 2.6ns. The measured pulse pairing error is less than 20ps. Measured jitter (1 sigma) is less than 40ps. The jitter and pulse pairing measurements

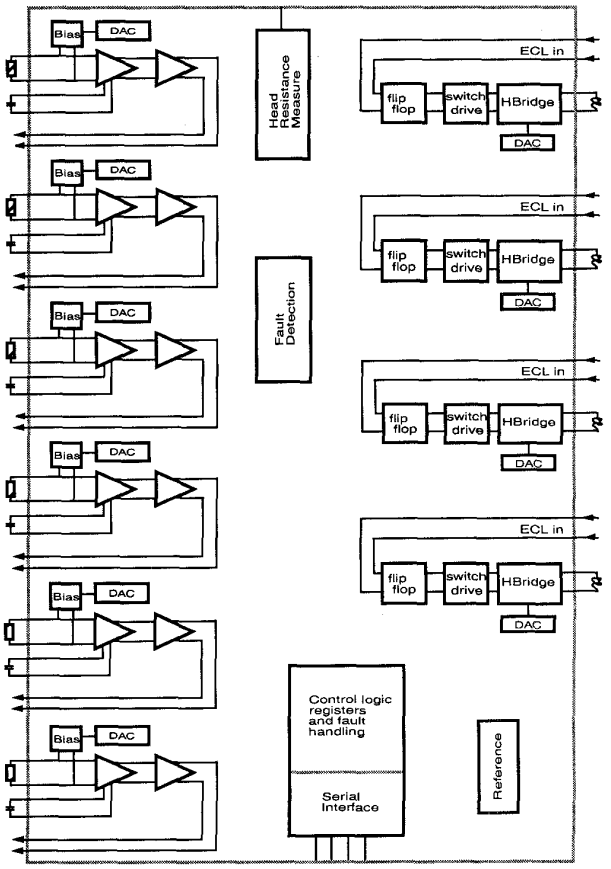

Fig. 5. Block diagram of IC

TABLE I
Summary of experimental results

Supply voltage	4.5V - 5.5V
Die area	36mm^2
Process	1.2μm BiCMOS
MR bias current	5.5mA - 15mA
Read bandwidth	>100MHz
CMRR	>40dB
Input referred noise R_{MR}=39 Ohms	1.0nV/sqrt(Hz) at 35MHz 1.55nV/sqrt(Hz) at 0.5MHz
Write driver rise time (45mA)	3.4ns with 300nH 2.6ns with 125nH
Write pulse pairing error	<20ps
Write jitter (1 sigma)	< 40ps

were similar with and without the flip-flop in the write data path. A die photo is shown in Fig. 8 .

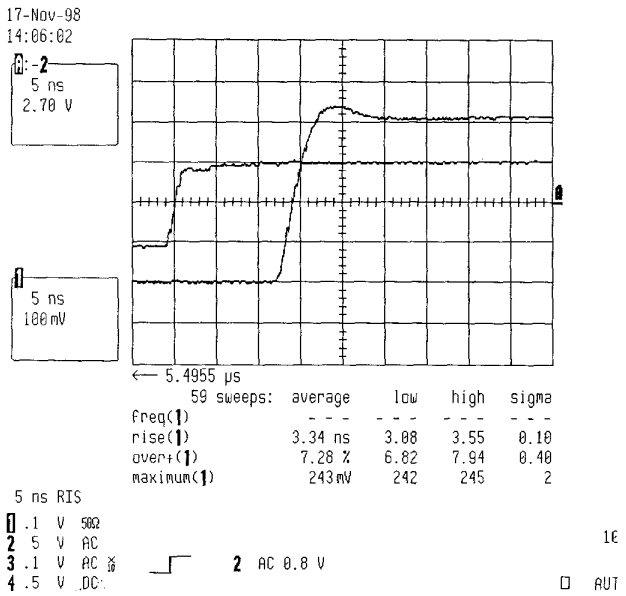

Fig. 6. Write driver rise-time with 45mA current and a 300nH load

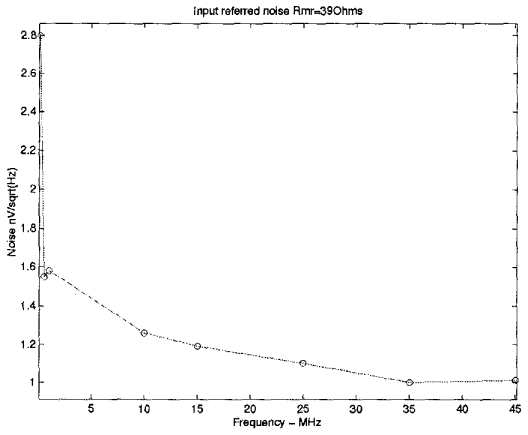

Fig. 7. Measured input referred noise versus frequency

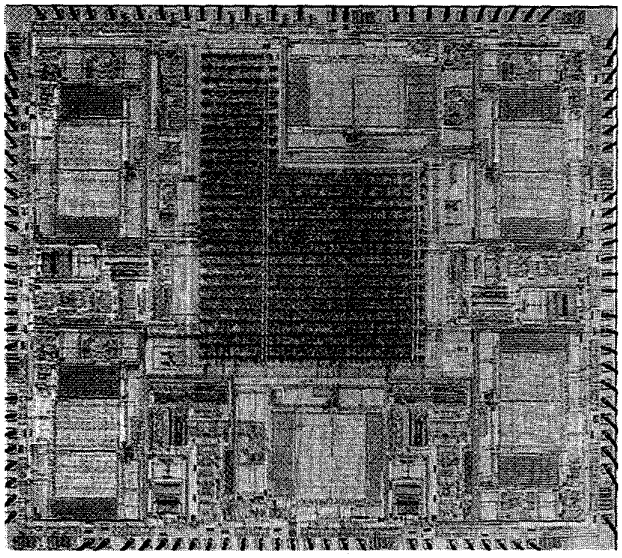

Fig. 8. Die Photo

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