FA 9.7: A 400MSample/s 6b CMOS Folding and Interpolating ADC

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A 6b 400MSample/s folding and interpolating CMOS ADC uses a low-impedance current-mode approach. Current division interpolation in the folders allows fast low-voltage operation. This interpolation together with a short aperture comparator, gives good performance for high-frequency inputs, without using a sample-and-hold. The ADC uses a single clock and its complement. The 0.6mm^2 CMOS converter, fabricated in a 0.5μm BiCMOS process dissipates 200mW from a 3.2V supply.

Communication systems and disk drive read channels require fast low-resolution analog-to-digital converters. Typically 6b of resolution is adequate. Sampling speeds ≥200MHz are common. In addition to the high sampling speed, power consumption and die area are critical. Because these applications are cost sensitive only standard CMOS processing can be used. For the system to benefit from advanced CMOS processes, the converter should function properly with low supply voltages.

A 200MSample/s 400mW CMOS 6b flash converter is reported [1]. Interpolation is used in a 6b 175MSample/s device [2]. A bipolar folding converter implemented in a 50GHz HBT process achieves a sampling rate of 4GHz [3]. A number of CMOS converters employing folding and interpolation, have resolutions in the 8-10b range and sampling speeds ≤100MSample/s [4, 5]. This work employs low-voltage interpolation and a low-kickback, short-aperture comparator to extend sampling speed to 400MSample/s.

Folding reduces the number of comparators compared to a flash type converter [4, 5]. Conceptually, the folding preprocessing operation maps the input signal in a modulo remainder fashion to a small range. The number of comparators is reduced by the degree of folding. Because folding is non-linear, parallel folders are added to reduce the required folding amplifier linear range. When enough folders are added, only the information concerning a single level crossing is extracted from each folding signal. Some of the folding signals can be derived through interpolation, reducing number of folders.

Because of the high-sampling speed, and the importance of low-power consumption, the circuitry is kept as simple as possible. The ADC uses a single clock and its complement. This avoids some of the problems of clock generation and distribution. In keeping with this design philosophy, and to ensure low-supply voltage operation, the number of devices in the signal path is minimized. Cascoding and additional biases are used sparingly.

Figure 1 is a block diagram of the 6b converter. The choice of the degree of folding is a tradeoff between the reduction in the number of comparators and the increased speed of the folding signals. A folding degree of 4 was chosen. Eight folding blocks generate eight folding signals. The number of folding signals is doubled by interpolating between the original eight folding signals. These sixteen folding signals drive sixteen comparators. The decoder suppresses bubble errors and translates the cyclic thermometer comparator code to a 5b binary representation. A coarse ADC determines the most significant bit. A synchronization block corrects for dc and transient offsets between the coarse and fine converters.

The folder is shown in Figure 2. For adequate transconductance, each differential pair is driven by a preamplifier. The folder outputs are differential currents. For speed, low impedance loads are used. A fold-by-4 folder normally requires 5 differential pairs. One pair is outside the input range and normally not exercised. Preamp power dissipation is reduced by almost 20%, using a single preamp to drive inactive differential pairs of all folders. A simple preamp with a resistor load is used. Resistor loads avoid the need for special bias lines. In addition, resistors match well and a linear resistance improves transient behavior.

Interpolation has been implemented with resistive dividers and by current division [4]. In this implementation, current division is incorporated within the differential pairs of the folder. The two transistors of each differential pair are replaced by two sets of four devices, dividing the current in four quarters (Figure 3). A quarter of the current from two adjacent folders is added to derive an intermediate interpolated folding signal. This differs from a previous scheme where complete folding signals are divided and interpolated. This scheme adds no extra nodes to the signal path, and keeps the circuit fast. Because no extra transistor voltage drops are added, the scheme works with low supply voltages.

The comparator is shown in Figure 4. An ECL-type structure is used because of its short aperture time. The cascode devices at the comparator inputs (M3 and M4) terminate the folder lines with a low impedance. The switches M5 - M8 divert the input current to the resistor loads during tracking ($\overline{Ck}$) and to the cross-coupled devices M9 and M10 during the latching phase (Ck). Because a constant current flows through the comparator, the folders are little disturbed when the comparators change between tracking and latching modes.

Despite its inherent advantages, this comparator structure presents design problems. The comparator output is valid for less than one half clock cycle. The output signal amplitude is insufficient to drive a CMOS logic stage. And most seriously, the comparator is extremely sensitive to kickback from subsequent stages. To overcome these problems, two resetable differential amplifiers couple the first stage to an unclocked latch (Figure 5). The output of both amplifiers is pulled low during $\overline{Ck}$, this reduces hysteresis. An additional slave latch (not shown) reduces the risk of indecision or metastability.

The design is fabricated with a 0.5μm BiCMOS process. Only CMOS devices are used. The minimum CMOS gate length is 0.42μm. Total power dissipation, including power used by the resistor ladder is 200mW from a 3.2V supply. At 400MSample/s with full power (2.3V) 1MHz input sinusoid, measured signal-to-noise-and-distortion ratio (SNDR) is 33.6dB (THD=44dB). At 450Msample/s SNDR drops to 32.9dB (THD=40.5dB). Figure 6 shows variation of SNDR with input frequency at 400MSample/s. The SNDR falls to 29.2dB (THD=33.6dB) for a full power 100MHz input. Using the technique described in Reference 5, at 400MSample/s, no metastability is observed in 2^8 samples. A micrograph of the 0.6mm^2 circuit is shown in Figure 7.

Acknowledgments:

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References: See page (429).

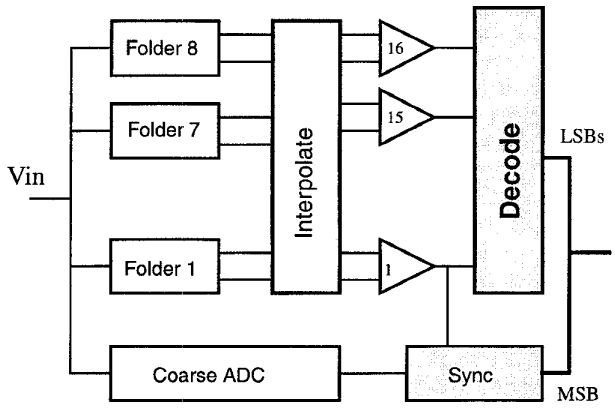

Figure 1: Converter block diagram.

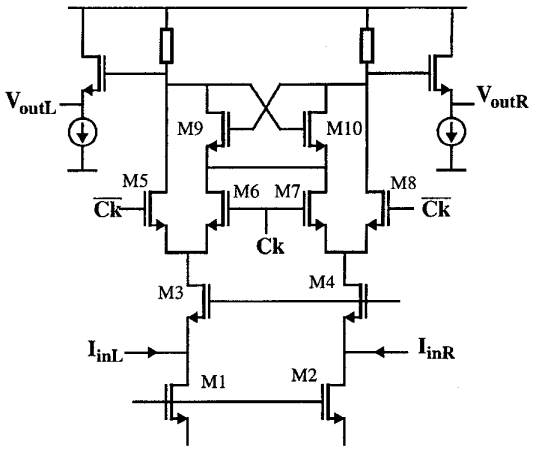

Figure 4: Comparator core. Inputs are currents IinL and IinR.

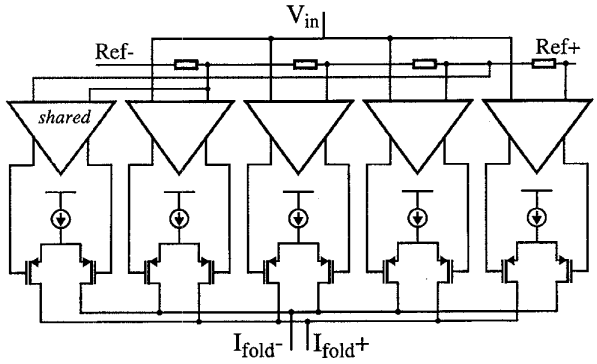

Figure 2: Simplified drawing of folder.

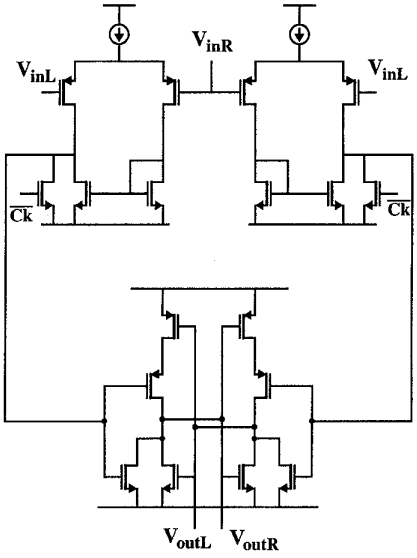

Figure 5: Comparator second stage.

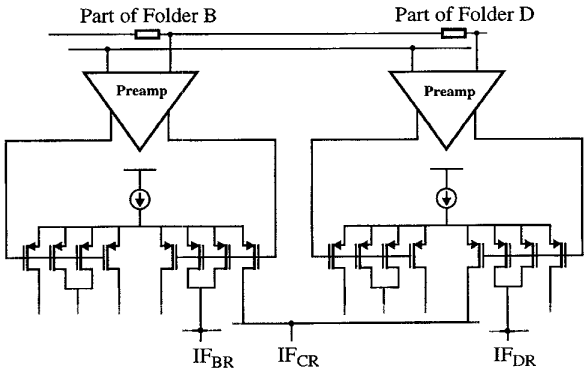

Figure 3: Two adjacent differential pairs from two folders. Divided currents are added to represent original (e.g., IFBR and IRDR) and interpolated currents (e.g., IFCR).

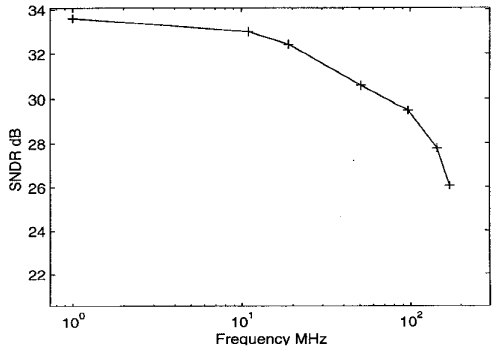

Figure 6: Variation of SNDR with input frequency at 400MSample/s.

Figure 7: See page 429.

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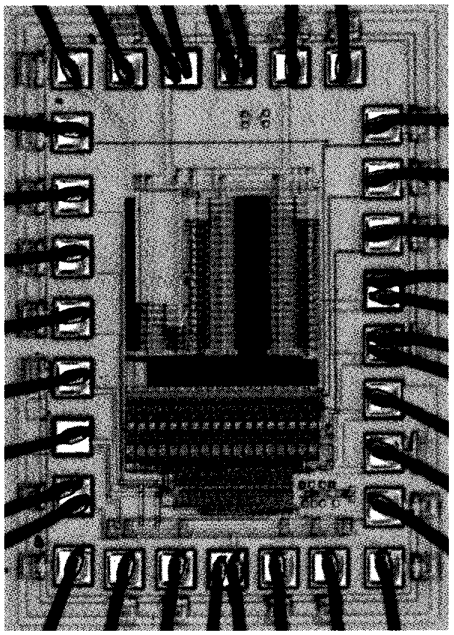

Figure 7: Die micrograph.