FA 16.2: CMOS Folding ADCs with Current-Mode Interpolation

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Folding and interpolating converters offer the speed of flash type devices but at a fraction of the area and power consumption. The performance of bipolar based folding converters has come to rival that of other topologies [1]. This work describes a folding architecture that is compatible with digital CMOS. For speed, the analog circuitry is fully-differential continuous-time current-mode and open loop.

In essence, folding reduces the number of comparators and hence the area, power consumption, and input capacitance of a flash type converter. Figure 1(a) shows how folding might be used in a 5b converter. The straight line represents the continuum of values within a converter range (in this example 32 levels). The dotted trace is the remainder after modulo division. This folded signal spans a smaller range, so fewer comparators are required to convert this signal with the same resolution. The number of decision levels is reduced by degree of folding, in this case by a factor of 4. Flash conversion of the folded input signal generates the 3 LSBs of the overall converter. The remaining bits, the two MSBs, represent the folding region and are determined by a separate coarse ADC.

In practice, the sawtooth folded wave form of Figure 1(a) is difficult to generate. A triangular waveform is usually more feasible, but its sharp corners tend to become rounded if the input voltage is changing with time. One solution is to use two parallel folding circuits, offset so that for all inputs one of the folders is operating in a reasonably linear region. The effective linear part can be small so it is better to use an even smaller region, adding more and more offset parallel folders. In the extreme case this linear region is reduced to a point. Each folder output is then compared to a single threshold. A complimentary folded signal can provide this threshold (Figure 1(b)).

Most bipolar folding blocks resemble a sine generator presented by Gilbert [2]. A similar MOS circuit is used here. To overcome the slowing effect of the large combined drain capacitance a current mode approach is adopted. Current outputs, instead of voltages, represent the differential folded signals (Figure 2). The performance of the circuit is further improved by the addition of a preamplifier. Each of the folder PMOS differential pairs is driven by a preamp. Using this technique, the aspect ratio of the differential pair can be reduced by the square of the preamp gain. Additionally, the preamp level shifts the input signal and limits feedthrough.

For finer resolutions the number of folders required becomes large, causing power consumption, complexity and area to become comparable to that of a simple flash. A solution is to generate many of the folded signals by interpolation. Interpolation has the added advantages of reducing the overall input capacitance and increasing the tolerance to mismatch in the folders.

In bipolar folding and interpolation, where the folded signals are voltages, interpolation is usually performed by resistive division. In this work current division techniques are applied to interpolate between folding currents. A simple current interpolator is shown in Figure 3. The original folding currents, If1 and If2, are divided in four by four identical nMOS transistors. A quarter of If1 is added to a quarter of If2 to form the intermediate interpolated signal. Two quarters of each input represent the original folding signals. In this example, one interpolated signal is formed so the degree of interpolation is 2. Higher degrees of interpolation can be realized at the expense of additional current-dividing transistors.

Part of the implementation is shown in Figure 4. The converter is comprised of a number of offset folding blocks, one of which is shown in the figure. The current sources, I_l and I_r, subtract the dc bias or common-mode component of the differential folding signals If1 and Ifr. Subtracting this offset improves interpolation accuracy. The remaining part of the folding current is interpolated with the help of current division. For the sake of simplicity interpolation of degree 2 is shown. Current mode comparators compare the differential interpolated folding signals.

Figure 5 shows the overall ADC implementation. A number of offset parallel folders generate differential folding signals. Interpolation increases the number of folding signals for comparison. The comparator outputs are decoded to determine the fine bits. Voting type error correction limits large errors [3]. A smaller coarse ADC determines the most significant bits. To reduce timing mismatch, the coarse ADC is built with the same folding, interpolation, and comparison blocks. Errors due to any remaining timing mismatch, between the coarse and fine converters, are suppressed by the Bit Sync circuitry.

A Monte-Carlo type simulator, based on Pelgrom's analysis, is used to explore effects of MOS device mismatch [4]. Simulations determine minimum device size and circuit parameters (for example the degree of folding). The design parameters for the 6 and 8b converters are summarized in Table 1. Error correction and decoding are implemented entirely on chip for the 8b converter. All logic and buffering is implemented with low-noise current-steering CMOS logic. The circuits are fabricated in a 1μm CMOS process. Ordinary MOS transistors are used throughout and gate poly is used to implemen the resistor strings. A micrograph of the 8b part appears in Figure 7.

The specifications for both converters are given in Table 2. The 8b converter was tested to a sampling rate of 100Ms/s. In the prototype lot, for a 40kHz input, the average SINAD is measured to be 45.1dB with a standard deviation of 0.7dB. Figure 6 shows the reconstruction of a 40kHz sinusoid sampled at 80MHz. The corresponding FFT is also given. The 8b ADC dissipates 250mW, more than 100mW of which is consumed by the digital logic and output buffering. For the prototype (at 80Ms/s) the input bandwidth is limited to about 6b at 3MHz. The 6b converter samples a 72kHz sinusoid at 150MHz with a SINAD of 34dB and dissipates 55mW. Both parts also function at 3.3V.

Acknowledgments

The authors thank P. Yee and T. Ng.

References

[1] van Valburg, J., R. van de Plassche, "An 8b 650MHz Folding ADC," ISSCC Digest of Technical Papers, Feb., 1992, pp. 30-31.

[2] Gilbert, B., "A Monolithic System for Analog Synthesis of Trigonometric Functions and their Inverses," IEEE J. Solid-State Circuits, vol. 17, no. 6, pp. 1179-1191, Dec., 1982.

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[4] Pelgrom, M. J. M., et al., "Matching Properties of MOS Transistors," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433-1439, Apr., 1989.

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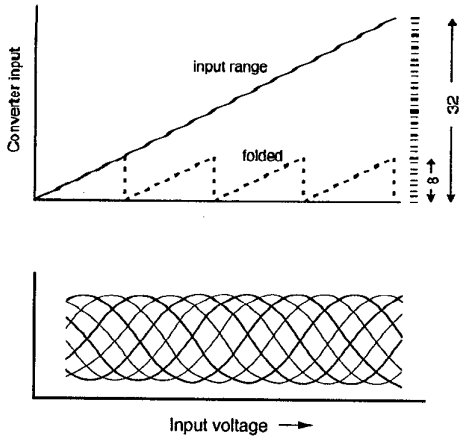

Figure 1: (a) Example, folding by 4 in a 5b converter, (b) offset parallel folders and compliments overcome rounding.

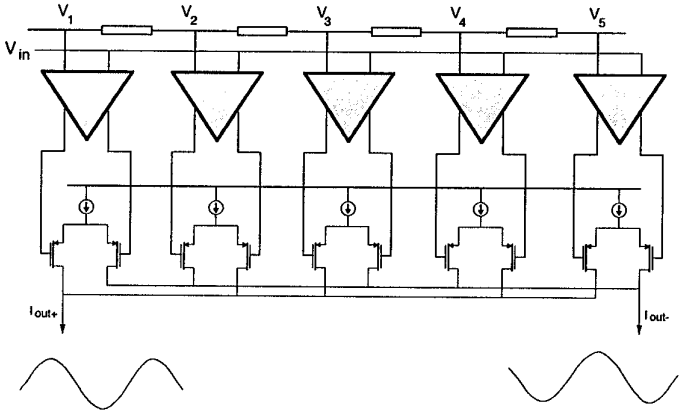

Figure 2: CMOS folder with preamps.

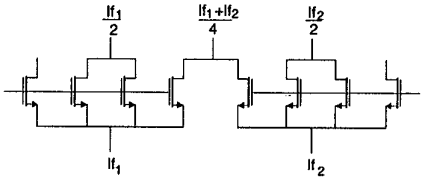

Figure 3: Current mode interpolation.

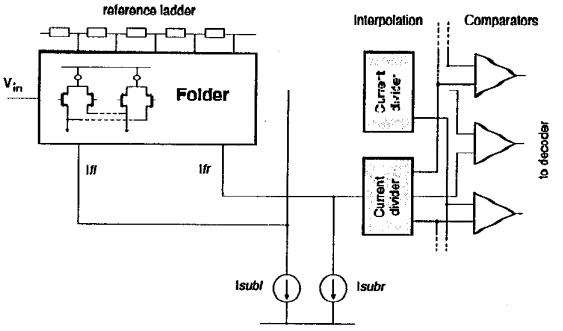

Figure 4: Part of implementation.

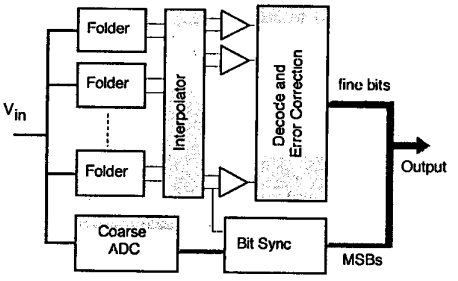

Figure 5: Block diagram.

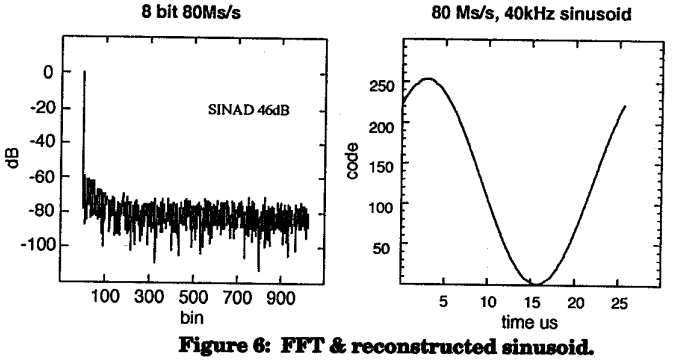

Figure 6: FFT & reconstructed sinusoid.

Figure 7: See page 378.

	8b	6b
Folding degree	8	8
Folders	8	4
Interpolation	4	2
Folding bits	5	3
LSB size	10nV	<40mV

Table 1.

	8b	6b
Sampling speed	100MHz	150MHz
SINAD at max Fs	45dB	34dB
Input Cap	5pF	2.5pF
Area	4mm²	2mm²
Power	250mW	55mW
Supply	3.3-5V	3.3-5V

Table 2.

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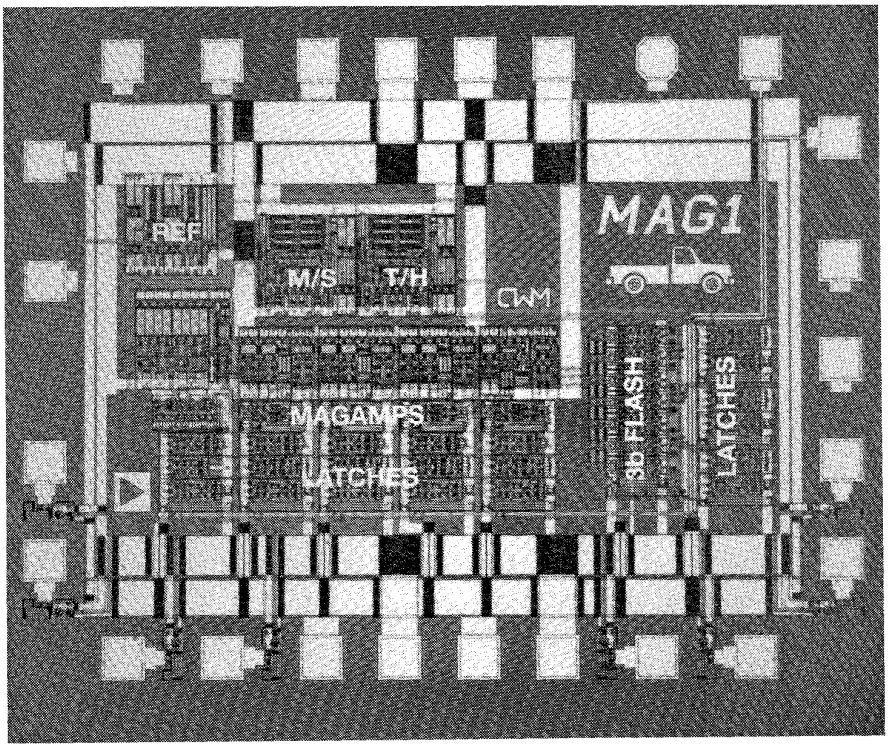

Figure 6: Chip micrograph.

FA 16.2: CMOS Folding ADCs with Current-Mode Interpolation

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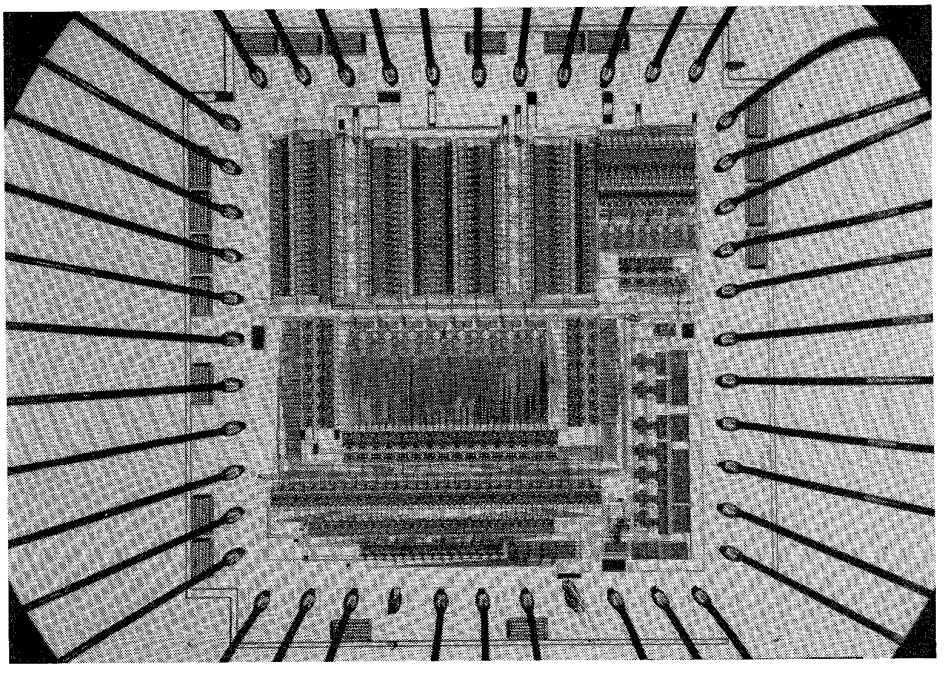

Figure 7: Chip micrograph.