A 1.2-μm CMOS Current-Controlled Oscillator

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Abstract—A simple, fully symmetrical, current-controlled CMOS oscillator is presented. The oscillator uses two grounded capacitors. This 5-V architecture permits relatively large capacitor voltage amplitudes, thus minimizing jitter. However, the design also operates with power supply voltages as low as 3 V. Because there are no special capacitor requirements, the design is compatible with standard scaled digital CMOS processes. The use of a double differential latching comparator allows high-speed operation with good control linearity. The circuit was successfully fabricated using a 1.2-μm CMOS process.

I. INTRODUCTION

CONTROLLED oscillators are extremely useful circuits, with particular use in telecommunications. Controlled oscillators are an integral part of phase-locked loop (PLL) circuits. Clock or timing recovery circuits are essential for data communications and storage systems. PLL circuits can also be used for FM modulation and demodulation. Controlled oscillators have been used to a lesser extent in sensor telemetry. Depending on the application, two performance parameters are critically important: low oscillator jitter is important in clock recovery, whereas control linearity is of greater interest in FM modulation. The highest possible maximum oscillator frequency is often desirable.

In a relaxation oscillator both the maximum speed and the control linearity are related to the total switching and comparison speed. Control linearity can be improved using negative feedback techniques [1] or compensation [2]. However, such schemes not only add complexity but also may affect the dynamic capabilities of the oscillator. Furthermore, because the maximum oscillation frequency is ultimately determined by the comparison and switching delay, it is important that this delay be minimized.

Jitter, or random variations in oscillator period, has its origins in circuit noise. It has been shown that jitter is reduced by maximizing the capacitor voltage waveform amplitude [3], [4]. The amplitude can be increased by increasing the rail voltage, but this is usually neither desir-

able nor practical. In fact, to be compatible with modern processes, circuits must use lower, not higher, voltages. Efforts to reduce jitter thus must concentrate on reducing circuit noise, and maximizing the capacitor voltage amplitude for a given power supply voltage.

Bipolar controlled relaxation oscillators are usually based on the emitter-coupled multivibrator. These circuits offer high speed and excellent temperature stability [5]. However, the high power consumption of these circuits renders them unsuitable for some applications. Furthermore, MOS or CMOS compatibility is required in many mixed-signal integrated systems.

Various MOS- or CMOS-controlled oscillator architectures have been proposed. For example, a monolithic controlled sinusoidal oscillator has been reported [6], and a number of high-speed CMOS-controlled ring oscillators (200–300 MHz) have been described [7], [8]. However, such circuits usually exhibit poor control linearity and are sensitive to device parameter variations.

Wakayama and Abidi described a 30-MHz CMOS voltage-controlled relaxation oscillator [4]. By employing a linearizing negative feedback loop, this VCO achieved very good control linearity. The disadvantages of such a scheme have already been mentioned. In this oscillator a floating-capacitor technique is utilized to extend maximum amplitude. Because node voltages in excess of the supply voltage are a feature of this design, this scheme is unsuitable for small geometry processes, where the supply voltage is often close to the maximum permissible voltage.

The advantages of using grounded capacitors in relaxation oscillators have been stated in [9]. A very high-speed controlled NMOS relaxation oscillator, implemented in a 0.75-μm NMOS process, was described by Banu [10]. This submicrometer circuit implemented grounded timing capacitors using only parasitics and used simple digital latches, not precise analog comparators and a latch, to control charging. In this way, speeds of several hundred megahertz were achieved, but at the expense of capacitor switching voltage inaccuracy, and inconsistency.

A general-purpose current-controlled relaxation oscillator is described in this paper [11]. The circuit allows relatively large capacitor voltage waveforms and so minimizes jitter. However, it is also compatible with present and future low-voltage fine-geometry CMOS processes. Additionally, because the circuit has no special require-
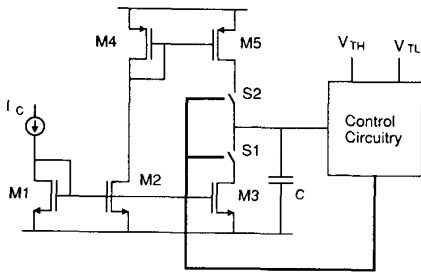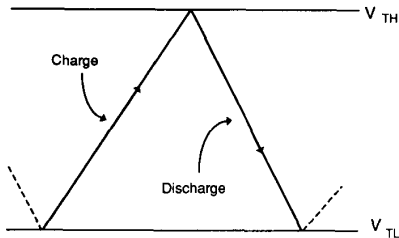
Fig. 1. Standard CMOS relaxation oscillator.

Fig. 2. Capacitor voltage waveform of standard oscillator.

ments for linear capacitors, it can be implemented on a standard digital CMOS process.

II. MOTIVATION—A STANDARD CONTROLLED RELAXATION OSCILLATOR

In the simple CMOS grounded-capacitor, current-controlled oscillator shown in Fig. 1, a timing capacitor C is alternately connected to charging and discharging currents. The control current I_C is mirrored to the NMOS device $M3$ to supply the discharging current or to $M5$ to supply the charging current, also nominally equal to I_C. Assume initially that switch $S2$ is closed. The capacitor is charged until its voltage exceeds an upper threshold V_{TH}. When this occurs the control circuit opens switch $S2$, closes switch $S1$, and discharge begins. Discharging continues until the capacitor voltage falls below a lower threshold V_{TL} at which time the entire cycle repeats, resulting in the capacitor voltage waveform shown in Fig. 2. If switching delay is ignored, then the oscillation frequency can be shown to be

$$f = \frac{1}{T} = \frac{2I_C/C}{V_{TH} - V_{TL}}. \tag{1}$$

This simple circuit suffers from several disadvantages. Because there are two thresholds, two reference voltages must be supplied. The fact that the capacitor is charged between two threshold voltages, which for practical reasons must be separated by about a volt from the supply rails, means that the amplitude of the capacitor voltage waveform is limited. In practice the PMOS charging and NMOS discharging currents will never be exactly equal. Furthermore, switchings at the ends of charging and discharging intervals occur at different voltages. This means that the desired 50% duty cycle is difficult to achieve.

III. DOUBLE-CAPACITOR OSCILLATOR

A double-capacitor oscillator, which overcomes many of the deficiencies of the simple oscillator, is described in this section. As can be seen in Fig. 3, traditional emitter-coupled bipolar oscillators (and similarly many CMOS oscillators) charge and discharge a single floating timing capacitor C_T. Although the unavoidable stray capacitances Cpl and Cpr do not form part of the timing capacitance, they nevertheless have an effect on oscillator timing. In order to overcome this problem, Sneep and Verhoven [12] and Banu [10] (in a MOS equivalent) replaced the single floating capacitor with two grounded capacitors. The parasitics are now in parallel with the timing capacitor. To minimize capacitor size in an effort to maximize oscillator speed, Banu used the parasitics themselves as the two grounded capacitors. But whereas in Banu's circuit speed is optimized, the oscillator presented here uses a similar structure to increase capacitor voltage amplitude and to improve duty cycle and reproducibility.

In the simplified schematic of the double-capacitor oscillator (Fig. 4), the two comparators and the latch perform the functions of the control circuitry in the simple oscillator. The control current I_C is mirrored to the nominally identical PMOS devices $MO2$ and $MO3$ to provide identical charging currents for the identical capacitors $C1$ and $C2$. The control circuitry alternately connects each capacitor to the current sources for charging and to ground for discharge. However, we shall see that the period is determined only by the charging time.

To understand how the circuit works, assume that initially Q is low and its complement $\overline{Q}$ is high. The PMOS switch $MO4$ is ON, connecting $C1$ to its charging current source $MO2$; $C2$ is discharged directly to ground via the NMOS device $MO7$. $C1$ continues to charge until $V1$ exceeds V_{ref}. When this happens the output of the upper comparator goes high setting the latch, reversing the states of Q and $\overline{Q}$. Now $C2$ is connected to its charging source, and $C1$ is discharged rapidly to ground. $C2$ continues to charge until its voltage exceeds V_{ref}. When this occurs the latch again changes state and the entire cycle repeats. Neglecting switching delay, the output frequency is related to the control current by the following equation:

$$f_{ideal} = \frac{I_C}{2CV_{ref}}. \tag{2}$$

The capacitor voltage waveforms are shown in Fig. 5. The discharge switches ($MO5$ and $MO7$) are sized to ensure that discharge is always completed well before charging, so the period is determined solely by the sum of the charging times. Switching always occurs at the same voltage V_{ref}, and therefore because of symmetry, a 50% duty cycle is achieved. Floating capacitors, which are necessary in other architectures, are not required. Moreover, as parasitics and other nonidealities affect both capacitors equally, the duty cycle is not altered. In fact, nonlinear MOS gate capacitors could be used without det-
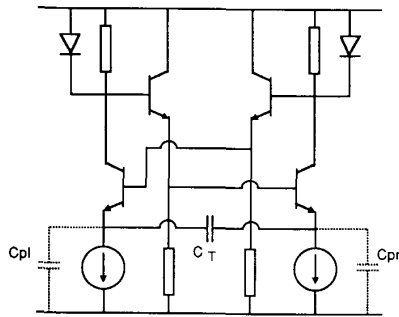
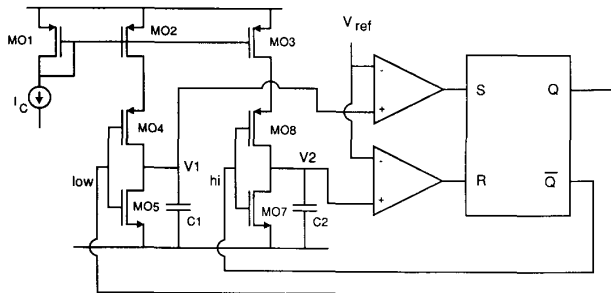Fig. 3. Emitter-coupled bipolar oscillator.

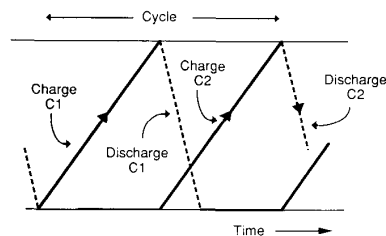Fig. 4. Double-capacitor oscillator structure.

Fig. 5. Capacitor voltage waveform of double-capacitor oscillator.

Fig. 6. Effect of switching delay on control characteristic.

rimental effects. Furthermore as the capacitors are charged from ground potential to V_{ref}, which depending on the specifics of design may be close to V_{DD}, relatively large capacitor voltage amplitudes are achievable. Jitter is further reduced by the absence of level-shifting circuitry.

IV. LATCH AND COMPARATOR CIRCUITRY

If the switching and comparison time delay is ignored, then the output frequency is directly proportional to the control current. As illustrated in Fig. 6, this delay time introduces nonlinearity in the control characteristic. If the total delay time per cycle is represented by T_d, then the actual frequency can be related to the ideal one by the following equation:

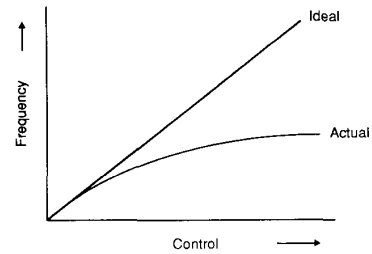$$f_{actual} = \frac{f_{ideal}}{1 + T_d f_{ideal}}. \tag{3}$$

Clearly, to improve linearity and increase the maximum oscillation frequency, T_d should be minimized.

During the comparison and switching delay, charging continues so that the capacitor voltage overshoots the reference value. This is illustrated in Fig. 7. At high speeds the capacitor voltage ramp rate is greater so that for a given delay t_d the overshoot is also greater. However, the increased comparator overdrive speeds up comparison so that in effect delay time is less at higher frequencies. With a single capacitor oscillator the situation is more complicated. If the capacitor voltage overshoots the reference value by V_O, then additional time is also required during the discharge cycle to discharge this overshoot. If both charging and discharging currents are equal, the total time delay at the end of each half cycle will equal $2t_d$. With the double-capacitor oscillator, as the oscillation period is determined solely by charging time, the additional time required to discharge the overshoot does not add to the oscillation period.

In order to improve oscillator linearity, Wakayama and Abidi combined the comparison and latching functions in a double-differential latching comparator [4]. A simpler but equally effective variant is described here. The principle of the double latching comparator can be understood by examining the operation of the single latching comparator, shown in Fig. 8. MOSFET's $M2$, $M3$, $M4$, and $M6$ resemble the differential pair and active load of a classical CMOS differential gain stage. The extra components, resistor R and NMOS transistor $M5$, give the comparator latching capability. In the figure, the right-hand input to the comparator is connected to the reference voltage V_{ref}. A capacitor C is being charged by a current source I. The capacitor is also connected to the gate of $M2$, that is to the left-hand comparator input. Assume that initially X is low ($M5$ is OFF) and $V1$ is less than V_{ref}. In this state, there is no current flowing through R so that the diode-connected MOSFET $M4$ generates a gate voltage for $M6$, in current mirror fashion. As the capacitor is charged, $V1$ rises, and when eventually $V1$ becomes greater than V_{ref}, the current through $M3$ becomes greater than that flowing through $M2$. The voltage at node X rises turning on $M5$, which results in current flow through R. The voltage drop across R reduces the gate drive on $M6$
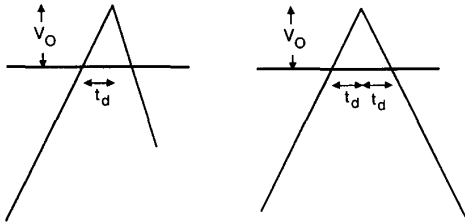
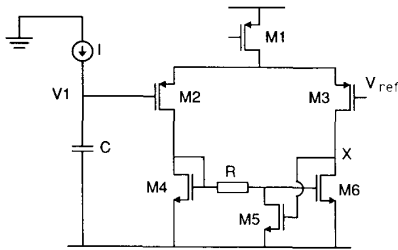Fig. 7. Effect of overshoot in a double- and single-capacitor oscillator.

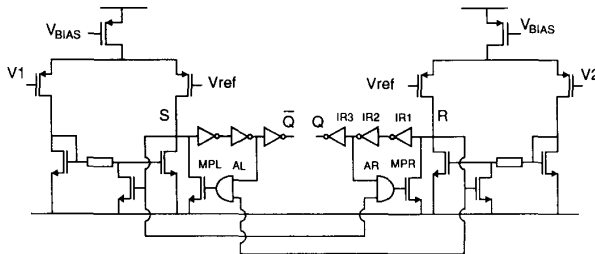Fig. 8. Single latching comparator.

Fig. 9. Simplified schematic of double-differential latching comparator.

Fig. 10. Double-differential latching comparator circuit.

and so causes X to rise further. Because of the feedback action, X is quickly latched high.

Two such single latching comparators can be combined to form a double-differential latching comparator as shown in simplified form in Fig. 9. This circuit functions as the two comparators and the set–reset latch in Fig. 4. The differential pair inputs are connected to the reference voltage and to capacitor voltages $V1$ and $V2$. The additional logic circuitry shown in Fig. 9 forces one of the latching nodes R or S to be brought low once its opposite node is latched high. For example, assume S is low, R is latched high, and $V1$ is rising. Soon after $V1$ exceeds V_{ref}, S latches high. The high level propagates through the AND gate AR, and activates the pull-down NMOS MPR, which attempts to pull node R low. The inverters $IR1$ and $IR2$ connected to R serve two purposes: they buffer the logic level R, and also because of their finite speed provide sufficient delay to insure that node R is pulled down fully. Returning to the example, pull-down must continue only while node R is high, but if R is connected directly to the pull-down transistor (i.e., without delay), then the pull-
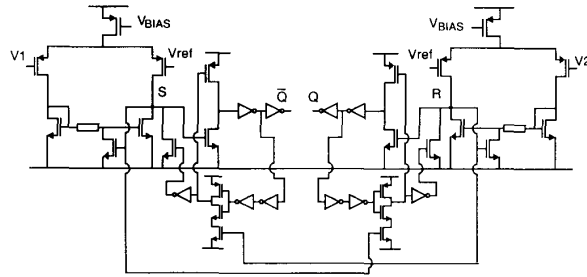
down transistor (MPR) might be turned off before node R is pulled down fully.

The double-differential latching comparator is shown in more detail in Fig. 10. In order to maximize speed, the capacitive loads on nodes S and R must be minimized. In contrast to a conventional CMOS inverter, the first inverter connected to nodes R and S presents only a single NMOSFET capacitive load to these nodes. Furthermore, pull-down is controlled by a three-FET dynamic NAND gate which also presents just a single MOSFET gate capacitance to nodes S or R.

V. JITTER ANALYSIS

Citing the definition used by Abidi and Meyer [3], jitter, or random fluctuations in oscillator period, may be expressed as

$$\text{Jitter} = \frac{\sigma_T}{\mu_T} \qquad (4)$$

where σ_t and μ_t are the standard deviation and mean, respectively, of the oscillation period. Jitter has its origins in circuit noise. To calculate jitter we refer the total circuit noise to a single equivalent noise source V_n, in series with the capacitor voltage, and at the input to the control circuit.

Abidi and Meyer showed that the variation in period σ_t can be calculated as

$$\sigma_t = \frac{\alpha \sqrt{6} V_n (\text{rms})}{S} \qquad (5)$$

where S is the slope of the capacitor voltage waveform and α is a constant of proportionality, valued between 0.5 and 1, depending on the spectral properties of the noise.

Thus, to estimate jitter in the double-capacitor oscillator circuit, we return again to a single latching comparator circuit connected as shown in Fig. 11. In this figure one comparator input is connected to V_{ref} and the second to a timing capacitor. This effectively represents operation of the entire circuit for one half cycle. Noise current through the capacitor can be ignored [3], so to calculate the magnitude of V_n, we need only examine the noise contributions of the devices in the latching comparator. Neglect-
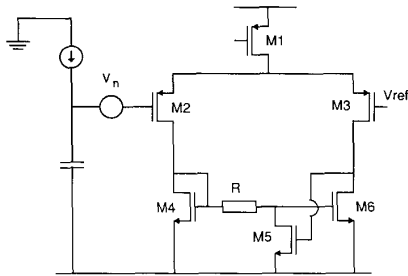

Fig. 11. Jitter analysis of oscillator.

ing the resistor noise, the total input-referred noise contribution of the comparator is

$$\overline{V_n^2} = \overline{v_{eq2}^2} + \overline{v_{eq3}^2} + \left(\frac{g_{m4}}{g_{m2}}\right)^2 (\overline{v_{eq4}^2} + \overline{v_{eq5}^2} + \overline{v_{eq6}^2}) \quad (6)$$

where $\overline{v_{eq1}^2}$ to $\overline{v_{eq5}^2}$ represent the equivalent gate-referred noise sources of the respective MOSFET's. Jitter can now be estimated using (5).

VI. MODIFICATIONS AND ADAPTATIONS

The performance and capabilities of the basic oscillator structure can be improved with some modifications. Because the reference voltage V_{ref} has a direct effect on the capacitor voltage amplitude, the linearizing or compensation techniques, discussed earlier, can be easily implemented. In these schemes the amplitude is adaptively controlled to maintain linearity. The oscillator can be converted to a voltage-controlled oscillator, simply with the addition of a voltage-to-current converter. Finally, to guarantee start-up, or to ensure start-up in a predetermined known state, additional power-up circuitry should be added.

VII. EXPERIMENTAL RESULTS AND DISCUSSION

The oscillator was fabricated on a 1.2-μm, 5-V, n-well, CMOS double-poly, double-metal process. The timing capacitors were implemented as high-linearity double-poly structures, and n-wells were used to implement the resistors. However, as already discussed, other capacitor structures could be used. The circuit occupies an area of only 50 000 μm^2. A photomicrograph of the integrated circuit is shown in Fig. 12.

A control current-to-frequency characteristic, measured with V_{ref} set at 1 V, is shown in Fig. 13. Frequency control over more than 6 octaves to a maximum of approximately 80 MHz is achieved. The time delay nonlinearity T_d varies form 12.2 ns at 20 MHz to 9.2 ns at 80 MHz. In other words, the total switching and comparison time is only 9.2 ns per cycle at 80 MHz. As already discussed, the delay time is less at high speeds because of increased comparator overdrive. With this design, capac-
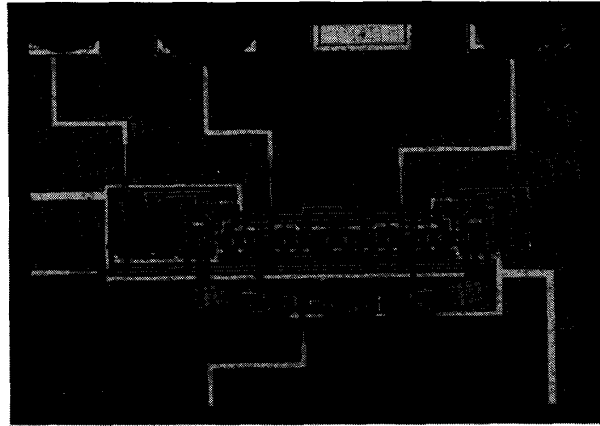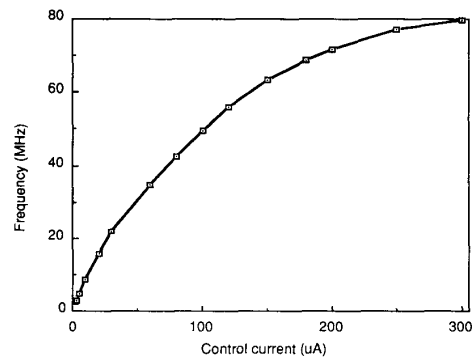

Fig. 12. Oscillator photomicrograph.

Fig. 13. Control-to-frequency characteristic of oscillator.

itor voltage waveforms with amplitudes in excess of 3.5 V are feasible. Because the comparator bias MOSFET's were biased in their linear regions, T_d was also found to increase with waveform amplitude. Simply replacing the PMOS bias FET's with larger devices operating in saturation should eliminate this variation.

Calculations indicate an input-referred noise for the latched comparator circuit of 28 nV / $\sqrt{Hz}$. If we estimate the noise bandwidth to be 100 MHz then (5) predicts oscillator jitter of approximately 140 ppm for a 2.5-V capacitor voltage amplitude. Timing jitter was also determined by measuring the deviation in oscillation period with a 400-MHz oscilloscope. At 400 kHz with the capacitor voltage amplitude set at 2.5 V, jitter was measured to be under 160 ppm. This compares favorably with the value of 100 ppm reported by Wakayama and Abidi for a 5-V amplitude capacitor voltage waveform [4].

With V_{ref} set at 1.5 V, the temperature coefficient of a 10-MHz output signal over a -20 to $120°C$ range was measured to be 90 ppm/$°C$. For comparison Kato et al. [5] report a temperature coefficient of less than 50 ppm/$°C$.

TABLE I
CIRCUIT CHARACTERISTICS

Nominal supply voltage	5 V
Minimum supply voltage	2.8 V
Die area	50 000 μm^2
Jitter	< 160 ppm
Temperature coefficient (10 MHz)	90 ppm/°C
Maximum oscillation frequency	> 80 MHz
Power dissipation (80 MHz)	20 mW

The oscillator duty cycle is determined by component matching, in particular matching of the timing capacitors, charging current sources, and of comparator input offset. For large voltage amplitudes the effect of comparator offset mismatch and capacitor value mismatch is overshadowed by current source mismatch (> 1%). Replacing the two current source PMOS devices (MO2 and MO3 in Fig. 4) with one single PMOS device of the same size, so that a single charging current is now steered alternately to the each capacitor, would eliminate this mismatch.

The circuit's structure permits operation at supply voltages much less than the nominal 5-V value. In testing, correct operation was observed with the power supply voltage as low as 2.8 V.

VIII. CONCLUSION

A 5-V current-controlled oscillator suitable for fine-geometry CMOS has been described. The oscillator was implemented in an analog process; however, because the circuit has no special capacitor requirements, it is equally suited to a digital process. To minimize jitter, the oscillator structure permits large capacitor voltage waveform amplitudes. The use of a high-speed double-differential latching comparator allows fast operation with high control linearity. The characteristics of the circuit are summarized in Table I.
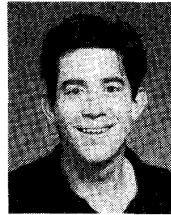
ACKNOWLEDGMENT

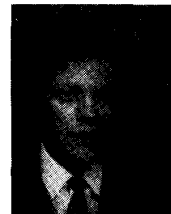The authors would like to thank Prof. D. J. Allstot for his advice and encouragement.

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Sverre U. Lidholm received the Ph.D. degree in electrical engineering from Chalmers University of Technology, Sweden, in 1977.
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