Oversampled Analog-to-Digital Converters

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Current state-of-the-art CMOS integrated circuit (IC) processes are ideally suited to implementing digital circuits; but they do not deliver the precision and accuracy required for high-resolution analog design. This is because the transistors have poor analog properties (such as linearity and gain) and the shrinking of the supply voltage makes the matter worse. The Analog-to-Digital Converter (ADC) is a key analog component in most applications. Thus, new techniques need to be developed to design ADCs in these new IC processes. Furthermore, the performance requirements (in terms of resolution, speed, and power) of such ADCs also increase with newer applications. This work involves the use of oversampling techniques to trade speed for accuracy. Sigma-delta (or oversampling) ADCs have been used traditionally for low-bandwidth, high-accuracy applications, and trading speed for accuracy. This work explores the use of over-sampling in high-speed applications.

A 14b 23MS/s ADC, that pipelines a 2nd order resetting ΣΔ modulator with a 10b cyclic ADC and requires no front-end S/H, was developed. The architecture uses a resetting ΣΔ modulator at the front-end for accuracy and a cyclic ADC at the back-end for residual error quantization. This calibration-free ADC achieves no missing codes, 87dB SFDR and 11.7b ENOB. Fabricated in 0.18μm CMOS with a core area of 0.5mm², it consumes 48mW from a 2V supply. This project is supported by an NSF CAREER grant.