

# ECE Final PhD Defense

## Nicholas Collins

### Mismatch-Immune Successive- Approximation Techniques for Nanometer CMOS ADCs

Monday April 10, 2017  
9:00 am – 10:30 am • 3725 Beyster Bldg

**Chair:** Michael P. Flynn

#### **Abstract:**

During the past decade, SAR ADCs have enjoyed increasing prominence due to their inherently scaling-friendly architecture. Several recent SAR ADC innovations focus on decreasing power consumption, mitigating thermal noise, and improving bandwidth, however most of those using non-hybrid architectures are limited to moderate (8-10 bit) resolution. Assuming a nearly rail-to-rail dynamic range, comparator noise and DAC element mismatch constraints are critical but not insurmountable at 10 bits or less in sub-100nm processes. On the other hand, analysis shows that for medium-resolution ADCs (11-15 bits, depending on dynamic range), the mismatch sizing constraint still dominates unit capacitor sizing over the  $kT/C$  sampling noise constraint, and can only be mitigated by drawing increasingly larger capacitors.

The focus of this work is to extend the scaling benefits of the SAR architecture to medium and higher ADC resolutions through mitigating and ultimately harnessing DAC element mismatch. This goal is achieved via a novel, completely reconfigurable capacitor DAC that allows the rearranging of capacitors to different trial groupings in the SAR cycle such that mismatch can be canceled. The DAC is implemented in a 12-bit SAR ADC in 65nm CMOS, and a nearly 2-bit improvement in linearity is shown with a simple reconfiguration algorithm.

