

# CMOS Bit-Stream Band-Pass Beamforming<sup>1</sup>

**Michael P. Flynn and Jaehun Jeong**

Electrical Engineering and Computer Science

University of Michigan

Ann Arbor, Michigan, USA, 48109

**Abstract:** *We introduce a unique bandpass  $\Sigma\Delta$  based common module with reconfigurable, bit-stream based digital beam-forming (DBF). An array of bandpass  $\Sigma\Delta$  modulators accurately and efficiently digitizes the IF signals. Beam-forming is implemented directly through bit-stream processing of the fast, low-resolution bit-stream outputs of the quantizers of each bandpass  $\Sigma\Delta$  modulator. Fabricated in 65nm CMOS, the prototype DBF generates two beams from eight input elements. The prototype is the first IC implementation of IF DBF, occupies  $0.28\text{mm}^2$ , and consumes  $124\text{mW}$ .*

**Keywords:** Digital beamforming; bandpass  $\Sigma\Delta$  modulator CMOS; bit-stream processing.

## Introduction

Beamforming improves SNR, and enables spatial filtering of interferers in receivers. However, high power consumption, large area, and routing complexity are bottlenecks to implementing an efficient beamforming system, especially for large numbers of elements.

Digital beamforming (DBF) offers the highest accuracy and flexibility. Another significant advantage is that DBF can simultaneously form multiple beams. However, despite these advantages, the adoption of DBF has been limited by high power consumption and large die area due to the need for multiple high-performance ADCs and extensive DSP. For these reasons, DBF is largely confined to base station applications, and implemented with FPGAs [4] or in software [5]. IF DBF is even more compelling because it simplifies the receiver chain by moving the ADCs closer to the antennas, and allowing I/Q down-conversion to be accurately implemented in the digital domain. However, power consumption and die area of conventional high-speed ADCs are prohibitive.

We introduce a new power and area efficient ADC-digital co-design approach to IF DBF that combines continuous-time band-pass  $\Delta\Sigma$  modulators (CTBPDSMs) and bit-stream processing (BSP). An array of compact ( $0.03\text{mm}^2$ ), low-power ( $13.1\text{mW}$ ) CTBPDSMs directly digitizes  $260\text{MHz}$  IF signals from eight input elements. DBF is directly performed on the over-sampled, un-decimated low-resolution outputs of the CTBPDSM array.

This new approach synergistically combines the direct digitization of the IF signals by an array of bandpass  $\Delta\Sigma$

modulators and the direct bit-stream processing of the outputs of these modulators to achieve filtering and beam-forming. A bandpass  $\Delta\Sigma$  modulator is an oversampled noise-shaping analog-to-digital converter that directly digitizes an IF signal. Continuous-time bandpass  $\Delta\Sigma$  modulation is ideal for the common module because:

- IF signal is directly and efficiently digitized without the need for down-conversion.
- The problems of an analog I/Q mixing (e.g. for effective image rejection) are avoided since down-conversion is implemented in the digital bit-stream domain.
- Oversampling is ideal for advanced CMOS because it trades speed for resolution.
- The anti-alias filtering requirements are greatly relaxed with continuous time bandpass modulators and these modulators can also implement filtering of out-of-band interferers.

A  $\Delta\Sigma$  modulator uses noise-shaping and oversampling to achieve high resolution from the output of a fast low-resolution quantizer. In a conventional  $\Delta\Sigma$  ADC, the bit-stream output generated by the high-speed quantizer is filtered and decimated to achieve the overall high-resolution ADC output. Instead, in this research we eliminate this extensive digital processing and implement beam-forming in the bit-stream domain. This novel bit-stream processing approach has the following advantages:

- The large overhead of filtering and decimation is eliminated.
- Bit-stream processing is ideal for digital down-conversion and beam forming.
- Bit-stream processing is highly amenable to reconfiguration because bit-stream processing operations are simple (e.g. AND gates).
- Advanced CMOS process nodes are ideal for fast bit-stream processing.

The bit-stream processing operates on the bit-stream outputs of the modulators to directly generate one or more down-converted, formed beams. This beam-forming is both highly accurate and flexible.

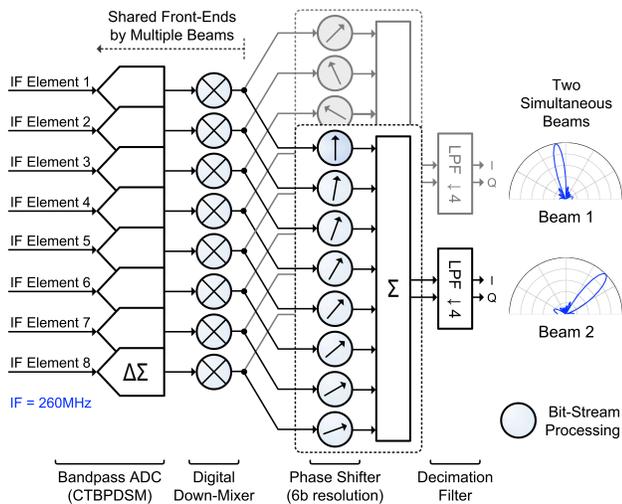
The unique combination of CTBPDSMs and BSP has several advantages. First, the CTBPDSMs efficiently digitize the relatively high-frequency IF signals, while the continuous-time architecture relaxes the anti-alias filter requirements, simplifying the RF front-end design. Second,

<sup>1</sup> This paper is based on [1], presented at IEEE RFIC 2015.

with direct IF sampling, most of the signal processing, including digital down-conversion (DDC), is carried out in the digital domain, and I/Q mismatch effects are minimized. Third, over-sampling and noise shaping in the CTBPDSMs enable a high SNR with a relatively low quantizer resolution (i.e. 5-level digital output). We take advantage of the very low word width to implement energy-efficient BSP arithmetic. Fourth, since BSP is directly performed on the over-sampled, un-decimated outputs of the CTBPDSMs, decimation filtering, a high-cost operation, is needed only once for the final output.

Combined with the CTBPDSMs, our prototype DBF IC performs band-pass filtering in both spatial and frequency domains. The narrowband nature of the CTBPDSM is ideal for phase-shift beamforming of narrowband signals.

### Overview

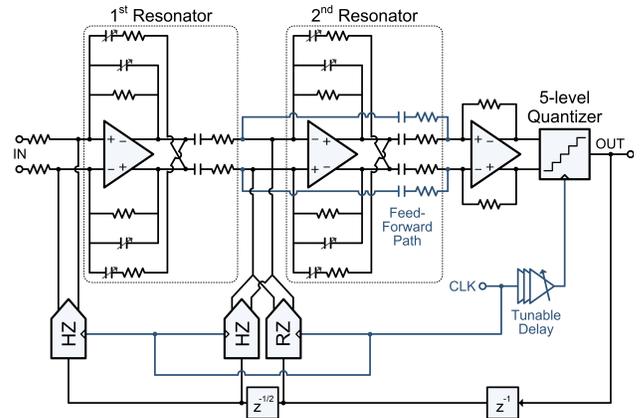


**Figure 2.** Overview of 8-element 2-beam prototype

A block diagram of the 8-element, 2-beam prototype DBF IC is shown in Fig. 1. Eight CTBPDSMs directly digitize 260MHz IF signals from eight input elements at 1040MS/s over a 20MHz bandwidth. The 5-level digital outputs of the CTBPDSMs are down-mixed, and phase-shifted by multiplication with programmable 6b complex weights. In this approach, the 5-level digitized signals are directly processed without decimation filtering for I/Q DDC and phase shifting. This novel BSP approach replaces bulky digital multipliers with simple multiplexers (MUXes), greatly reducing circuit complexity. Phase-shifted signals are summed to create 1040MS/s 10b beam outputs, which are low-pass filtered and decimated by four to produce the overall 260MS/s 13b I/Q outputs.

### Continuous-Time Bandpass $\Sigma\Delta$ Modulators

The circuit implementation of the 4<sup>th</sup> order CTBPDSM is shown in Fig. 2. Since an  $N$ -element digital beamformer requires  $N$  ADCs, the power consumption and area of



**Figure 1.** Implementation of the 4th order CTBPDSM

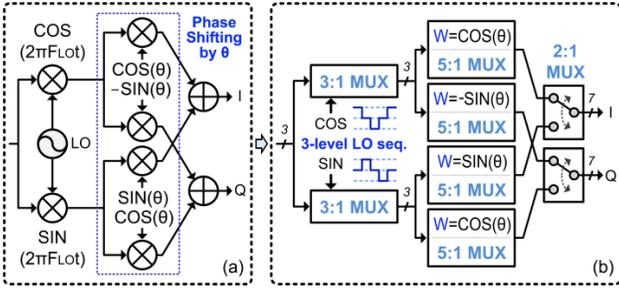
ADCs play a large role in the power consumption and area of the entire beamformer.

In the modulator, single op-amp resonators [6] consume less power, and are smaller than conventional LC-tank resonators. A high quality factor resonator is realized with a single op-amp by using positive feedback. The resonator center frequency of  $f_s/4$  (260MHz) simplifies the design of DDC. 4b tunable capacitors adjust the center frequency. A single feed-forward path around the 2<sup>nd</sup> resonator further improves efficiency. The modulator retains the 2<sup>nd</sup> order anti-alias filtering of the 1<sup>st</sup> resonator. The feed-forward path reduces the signal swing at the output of the 2<sup>nd</sup> resonator op-amp, relaxing power and linearity requirements. In addition, the feed-forward path removes a return-to-zero (RZ) feedback DAC to the 1<sup>st</sup> resonator input, reducing the input-referred noise of the modulator. Overall, the modulator has one RZ and two half-clock-delayed return-to-zero (HZ) current steering DACs.

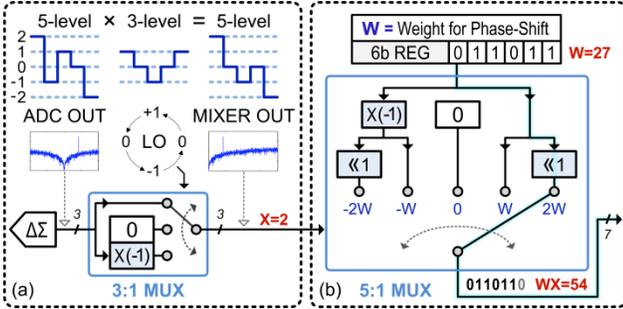
The output currents from the two resonators are summed together, converted to voltages, and quantized by a 5-level 1040MS/s flash quantizer. The low quantizer resolution facilitates MUX-based multiplication for phase shifting. Programmable trim currents calibrate comparator offsets. A 3b tunable delay corrects any excessive loop delay, aligning the sampling at the quantizer and feedback current triggering. The prototype beamformer contains eight CTBPDSMs. Each modulator consumes 13.1mW, and occupies only 0.03mm<sup>2</sup>, which is almost an order of magnitude smaller than the CTBPDSM in [6].

### Digital Down Conversion and Phase Shifting

Fig. 3(a) summarizes the mathematical operations of DDC and phase shifting by complex weight multiplication (CWM). The I/Q outputs of the down-mixers are weighted, and combined to generate phase-shifted I/Q outputs. In our BSP approach, the digital outputs of the CTBPDSMs are directly processed before they are low-pass filtered and decimated to enable MUX-based implementation of DDC and phase shifting. As a result, eight MUXes (Fig. 3(b)) replace six multipliers and two adders (Fig. 3(a)).



**Figure 3.** (a) Mathematical operations of DDC and CWM, and (b) MUX-based BSP implementation.



**Figure 4.** (a) DDC implemented with a 3:1 MUX and (b) CWM implemented with a 5:1 MUX.

**Digital Down-Conversion with a 3:1 MUX:** Choosing a CTBPDSM center frequency of  $f_s/4$  greatly simplifies the design of DDC [7], since the LO signals,  $\cos[n\pi/2]$  and  $\sin[n\pi/2]$ , are now represented by only three values (-1, 0, and +1). DDC (Fig. 4(a)) is performed with a simple 3:1 MUX: pass-through, zero, and sign-change. Moreover, after multiplication by the 3-level LO signals (-1, 0, or +1), the down-mixed 5-level CTBPDSM outputs are still represented by five levels (-2, -1, 0, +1, and +2).

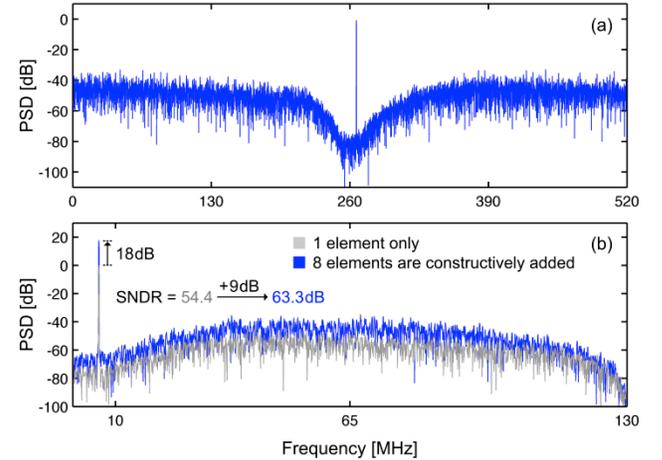
**Phase Shifting with a 5:1 MUX:** We expand the multiplier-less single-bit DSP, proposed more than two decades ago in [8] to 5-level streams. Since all five levels of the down-converted signals are powers of 2, only 1b left-shift ( $\ll 1$ ) and sign-change are required for multiplication. The 5-level output of the down-mixer determines the 5:1 MUX operation on the 6b stored weight (i.e. sign-change, zero, and 1b left-shift). In this way, a 5:1 MUX performs multiplication for phase shifting with 6b programmable weights. The result of this multiplication is a 7b output. In addition, since the 3-level I/Q LO sequences are alternately zeroes, only the I or the Q output of the down-mixer is non-zero at any time. Therefore, the two 2:1 MUXes simply implement the two adders in Fig. 3(a). Overall, the four multipliers and two adders required for phase shifting are implemented with 6 MUXes, greatly reducing complexity.

## Measurements

The 8-element, 2-beam DBF IC is fabricated in 65nm CMOS (Fig. 8), and occupies a core area of  $0.28\text{mm}^2$  ( $0.24\text{mm}^2$  for eight ADCs and  $0.04\text{mm}^2$  for the DBF

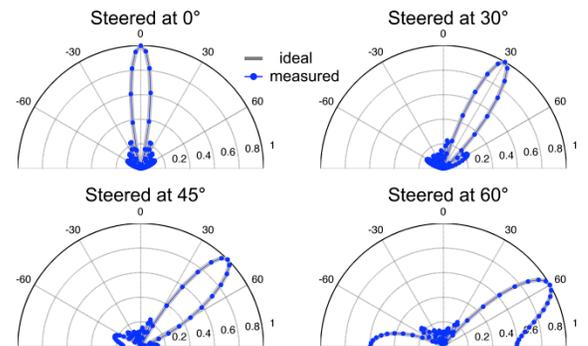
core). Each CTBPDSM consumes 13.1mW from a 1.4V supply. For a single CTBPDSM with a 266MHz input sinusoid, the average measured SNDR is 54.4dB over a 20MHz bandwidth (Fig. 5(a)).

The outputs of the eight CTBPDSMs are fed to the Verilog synthesized DBF core, which consumes 18.9mW from a 0.9V supply. When the eight CTBPDSM outputs are down-mixed, phase-shifted, and constructively added, the fundamental tone linearly increases by 18dB while element noise is uncorrelated, resulting in an SNDR of 63.3dB corresponding to a 9dB array improvement over a 10MHz bandwidth (Fig. 5(b)).

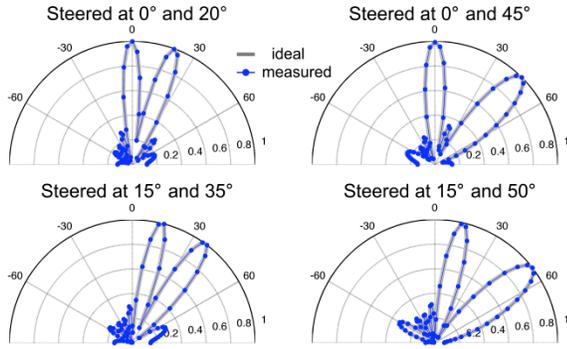


**Figure 5.** (a) Measured spectrum of the single CTBPDSM output (b) Measured spectrum of the beam output.

The prototype DBF IC produces two independent beams from eight input elements. Various weighting functions can be applied with 6b programmable weights. A simple phase-shift with a set of complex weights of  $e^{j(k\theta)}$  (where  $k = 0, 1, \dots, 7$ ) adjusts the delay in the  $k$ -th channel to create one main-lobe at a desired angle. Fig. 6 shows the measured single main-lobe beam patterns overlaid on ideal beam patterns. During measurements, eight synchronized direct digital synthesizers (DDSs) generate poly-phase sinusoidal inputs to mimic the received signals from an antenna array with  $\lambda/2$  spacing. The beam measurement step size is  $2.5^\circ$ .



**Figure 6.** Measured and ideal beam patterns (with one main-lobe).



**Figure 7.** Measured and ideal beam patterns (with two main-lobes).

Combining two single main-lobe responses creates a single beam with two main-lobes. This is easily done in the digital domain by using combined complex weights of  $(e^{j(k\theta_1)} + e^{j(k\theta_2)})/2$  (where  $k = 0, 1, \dots, 7$ ) at the cost of 6dB reduced array gain. The measured beam patterns with two main-lobes are shown in Fig. 7.

A second simultaneous beam can be configured with the same flexibility. The measured beam patterns show great consistency with the ideal patterns, which is difficult to achieve in analog beamforming (ABF).

## Conclusion

This paper describes the first IC implementation of IF DBF. The unique combination of CTBPDSMs and BSP avoids high power consumption and large area, which have prevented the low-cost implementation of DBF. Compared to ABF ICs [2, 3], the prototype DBF IC has more elements, more beams, better phase resolution, better array SNDR improvement, and has the advantages of the inherent accuracy and flexibility of digital processing. The power consumption per unit element of the prototype is only 6% of the FPGA implementation in [4].

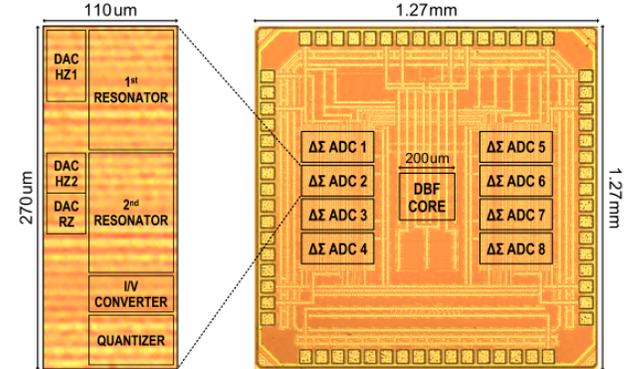
TABLE I  
PERFORMANCE SUMMARY AND COMPARISON

Metric	This Work
Beamforming	Digital
Number of	8
Number of Beams	2
IF Bandwidth <sup>(1)</sup>	20
Array SNDR [dB]	63.3
SNR Improvement	$g^{(2)}/g^{(3)}$
Phase Resolution	6
Power [mW]	124
Active Area [mm <sup>2</sup> ]	0.28
Technology	65nm CMOS

(1)for 1-element (2) measured (3) theoretically expected

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**Figure 8.** Die photograph.

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