A True Time Delay 16-Element 4-Beam Digital Beamformer

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***Abstract*—Large phased arrays are limited by inaccurate beam steering (squinting) and by distortion in analog-to-digital conversion. This paper introduces the first integrated digital true time delay beamforming receiver. The true time delay eliminates squinting, making it ideal for large-array wide-bandwidth applications. The beamformer incorporates a new current-steering DAC architecture providing a constant output impedance to improve ADC linearity. This significantly reduces distortion, leading to an SFDR improvement of 13.7 dB from the array. The prototype achieves an EVM better than -37 dB for 5 MBd 256-QAM and 512-QAM. The measured beam patterns are near-ideal for both conventional and adaptive beamforming. The prototype digital beamformer supports 16 antennas and 4 independent beams. It occupies only 0.29 mm^2 and consumes 453 mW.**

***Index Terms*—Digital beamforming, phased-array, linear array, delay line, receiver, MIMO, linearity, true time delay.**

I. Introduction

Digital beamforming (DBF) promises large (100s of elements) multi-beam arrays, but this promise has been limited by inaccurate beam steering over wide bandwidths and by distortion. This work provides efficient true time delay digital beamforming, allowing accurate beamforming for large arrays, over a wide frequency range. This true time delay design eliminates squinting and achieves near-ideal beam patterns even with adaptive beamforming techniques (i.e., adaptive null steering and tapering). The design builds on the power and area efficient interleaved bit stream processing (IL-BSP) concept introduced in [1]. It incorporates a new DAC architecture which reduces DAC distortion in the per-element continuous-time delta-sigma ADCs. This reduces distortion significantly in large arrays since these are limited by the inherent distortion of the element ADCs.

Current integrated beamformers approximate time delay by phase shift. This allows size and power efficiency [1], [2], but it is limited by poor beam steering away from the central frequency - a phenomenon known as squinting [3]. Fig. 1 shows the high-level architecture for a baseband phased-array, together with beam-squinting errors for a 1 GHz 16-element 100 MHz bandwidth phased-array. Notice that the central frequency (solid red) is steered accurately, but the beam squinting error can be as large as 18° for frequencies 50 MHz from the center.

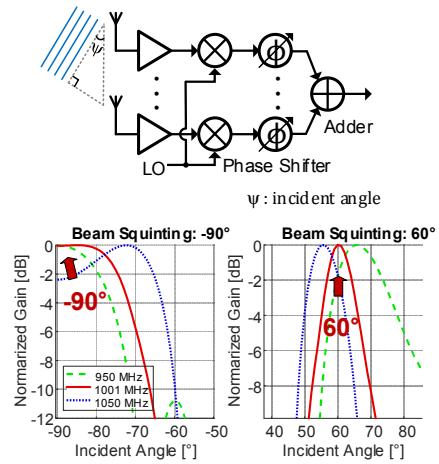

Fig. 1. System architecture of a conventional phase shifting beamformer and beam squinting errors of a 16-element 1 GHz-IF 100 MHz-BW beamformer.

Implementations of true time delay arrays are quite limited. RF true time delay beamformers replace phase-shifters with RF delay lines, but are limited to few hundred picoseconds time delay and suffer from delay variation over the input bandwidth [4].

II. True Time Delay Digital Beamforming

A. True time delay technique

We extend a baseband true time delay beamforming technique, originally proposed for acoustic bandpass beamforming in the 90's [5], to digital beamforming. A simple time delay at baseband by itself is not mathematically equivalent to a delay at RF. Instead, our DBF technique applies both a phase shift and a delay to the baseband I/Q signals to attain the equivalent of true RF time delay. We understand this approach by considering the relative delay of the signal at the *k*th element which is kτ, for a half wavelength antenna spacing, where,

$$\tau = \frac{\lambda}{2}\frac{\sin\psi}{c}, \qquad (1)$$

and λ is the wavelength of the carrier, ψ is the given beam incident angle, and c is the speed of the light.

Thus, the *k*th element receives:

$$R_k(t) = I_0(t+k\tau)\cos(\omega_c(t+k\tau)) - Q_0(t+k\tau)\sin(\omega_c(t+k\tau)) \qquad (2)$$

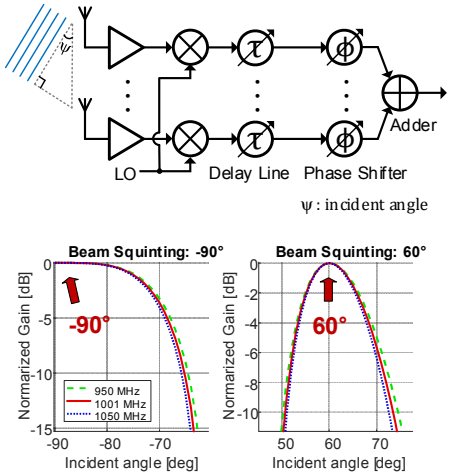

Fig. 2. System architecture and beam squinting errors of 16-element 1 GHz-IF 100 MHz-BW beamformers based on time delay with phase shifting.

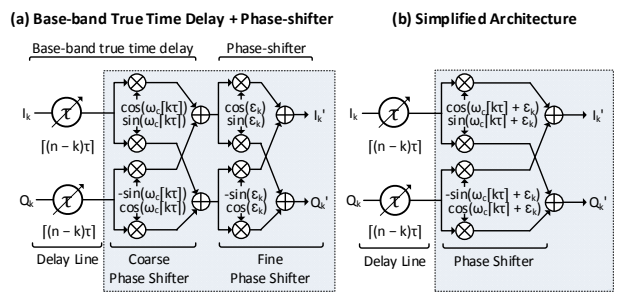

Fig. 3. A hybrid digital beamforming architecture combining true time delay and phase shifting.

where I_0 and Q_0 are the quadrature signals received at the 0th element. Reformulating, using some trig identities and matrix language, we obtain:

$$R_k(t) = [\cos(\omega_c t) \quad -\sin(\omega_c t)] \begin{bmatrix} \cos(\omega_c k\tau) & -\sin(\omega_c k\tau) \\ \sin(\omega_c k\tau) & \cos(\omega_c k\tau) \end{bmatrix} \begin{bmatrix} I_0(t+k\tau) \\ Q_0(t+k\tau) \end{bmatrix} \quad (3)$$

This expression has the form:

R_k = Carrier × Phase Shift × Delayed Baseband.

Our true time delay system shown in Fig. 2 removes the carrier term by down-mixing to baseband. It synchronizes the delayed baseband signals using an additional time delay of $-k\tau$, and finally, it undoes the phase shift by some complex weight multiplications (CWM).

B. Practical considerations

In practice, a causal system cannot implement a negative time delay $-k\tau$. We add a constant time delay $n\tau$ to each element, making all the delays, $(n-k)\tau$, positive. Also, the resolution of the time delay is limited by the rate of the digital stream. In our system, the digital time delay has a resolution of 500 ps. Thus, instead of the ideal time delay of $(n-k)\tau$, where n is the array size, we delay by the closest number of digital increments, which we denote by $\lceil (n-k)\tau \rceil$.

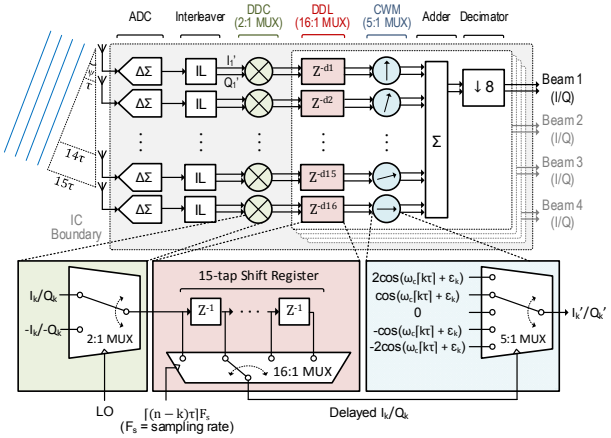

Fig. 4. System architecture of the true time delay interleaved bit stream processing (IL-BSP) digital beamformer.

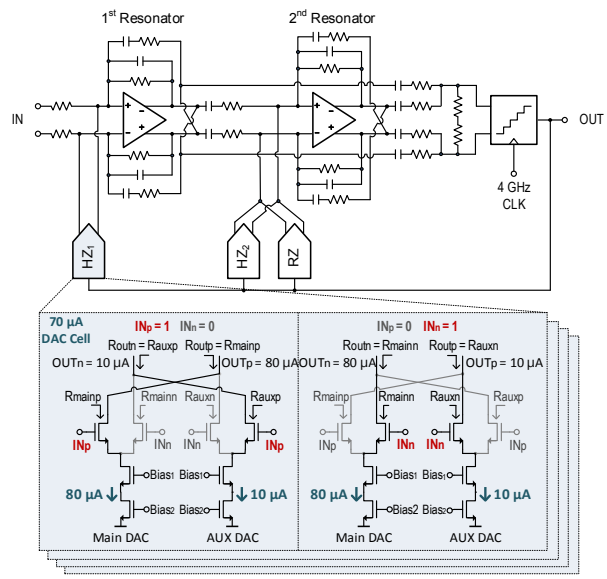

Fig. 5. Continuous-time bandpass delta-sigma modulator and a constant output impedance current steering DAC cell.

This shift differs from the ideal time delay by a small amount. To compensate for this small missing delay we introduce a small phase shift ε_k (Fig. 3(a)).

This hybrid approach combines the advantages of true time delay with the simplicity and compact size phase shifting. This phase shift combines with the phase shift of $\omega_c\lceil k\tau \rceil$ to give a total phase shift of $\omega_c\lceil k\tau \rceil + \varepsilon_k$. In our digital pipeline, we reduce to baseband, then delay by $\lceil (n-k)\tau \rceil$ increments, and shift phase by $\omega_c\lceil k\tau \rceil + \varepsilon_k$ (Fig. 3(b)). This trading of a small time delay error for a small phase doesn't introduce any noticeable squinting.

C. Implementation with Bit Stream Processing

We build on the interleaved bit stream processing approach in [1] to efficiently implement this true time delay technique. [1] uses an array of continuous time bandpass

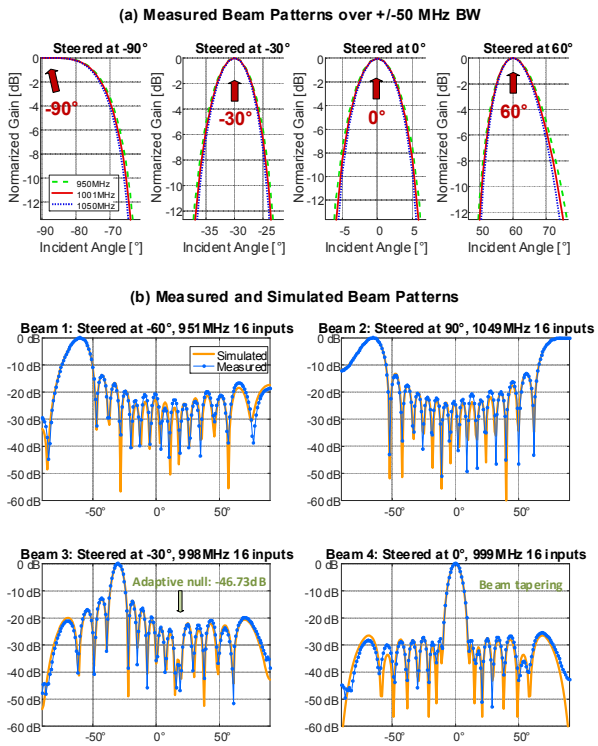

Fig. 6. (a) Measured beam patterns over +/- 50 MHz have no beam squinting error and (b) measured beam patterns are near identical to the ideal ones.

delta-sigma modulators (CTBPDSMs) to directly digitize high-IF signals, and implements phase shifting with bit stream processing (BSP). A disadvantage of the approach in [1] is that it is limited to conventional phase-shift beamforming. In this work, we take advantage of the fast sample rate of the CTBPDSMs to facilitate high-resolution digital time delay.

As shown in Fig. 4, 16 bandpass modulators generate 4 GS/s 5-level digital bit streams. Interleavers produce 2 GS/s quadrature I and Q signals. A digital down converter (DDC) down converts the digitized bandpass signal to baseband with a 2:1 MUX, using the 2-level (1 and -1) digital LO as the MUX select. The 16-level digital delay line (DDL) delays the signal with a 500 ps delay resolution from 0-7500 ps. Next, a 5:1 MUX, using the delayed quadrature signal as the MUX-select performs complex weight multiplication (CWM). Finally, the combined signals are decimated to 250 MS/s. Four copies of this processing produce four simultaneous independent beams.

III. Constant Output Impedance Feedback DAC

A big advantage of large arrays is that the array gain improves SNR and also attenuates uncorrelated errors (e.g. DAC transistor matching errors in the ADCs). However, the array cannot improve systematic non-linearity and therefore this limits the overall SNDR and SFDR of the beamformer. We tackle the dominant systematic

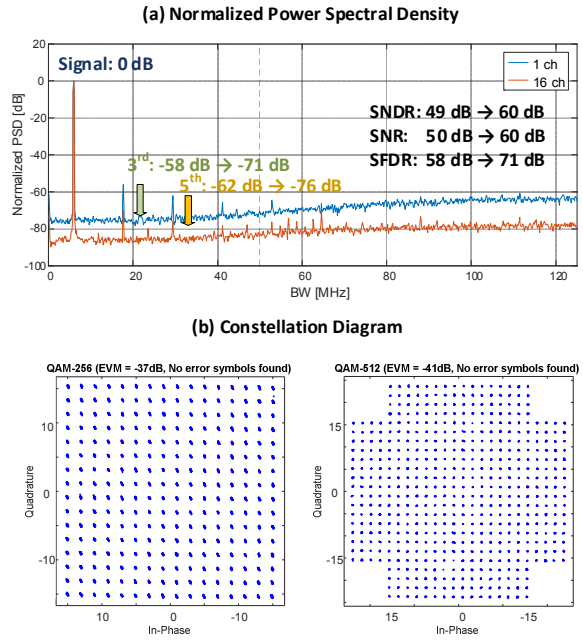

Fig. 7. (a) Normalized measured power spectral density plot for a single channel and entire array and (b) measured 256/512-QAM constellation for 16-element array.

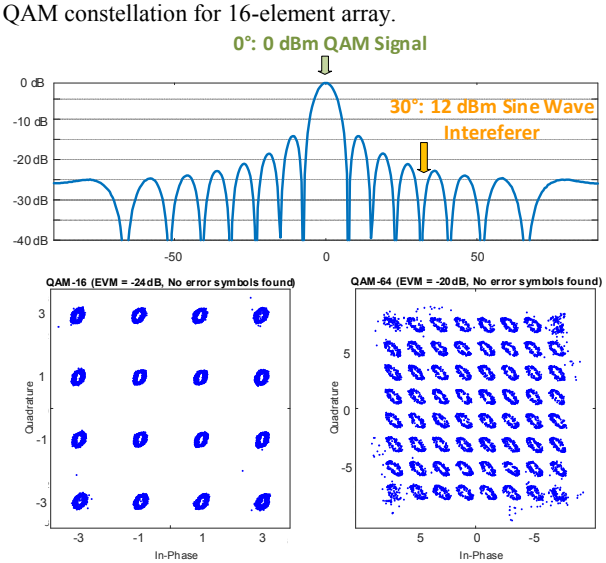

Fig. 8. Measured QAM constellations for 16-element array transmitted at 5 MBd with a large interference at 30° (Desired signal power: 0 dBm and interference power: 12 dBm).

nonlinearity of code dependent loading in the feedback DAC with a new DAC structure. Fig. 5 shows the CTBPDSM and DAC. The output impedance of a conventional current steering DAC is correlated with its input code. We introduce an auxiliary DAC to maintain a constant output impedance regardless of the input signal. As shown in Fig. 5, the input to the 10 µA auxiliary DAC is the opposite of the 80 µA main DAC, forcing one of the DACs to sink current at all times. This simple scheme

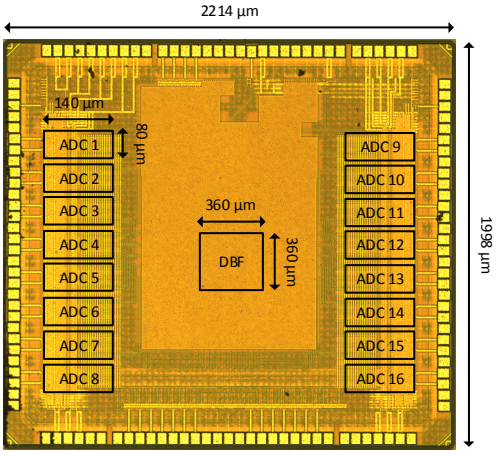

Fig. 9. Die Micrograph (2.214 x 1.998 mm^2).

eliminates the correlation between the output impedance and the input code and therefore improves SFDR by 6 dB.

IV. Measurements

Fig. 6(a) shows the measured beam patterns for input signals over the +/- 50 MHz input bandwidth from 1 GHz. With a measurement step size of 1°, the true time delay digital beamforming shows negligible squinting error. Furthermore, the measured 4-simultaneous beam patterns are almost identical to the simulated beam patterns (Fig. 6(b)). In these tests, beam 1 and 2 are programmed to steer the beam direction to -60° and 90°, respectively. The beam 3 and 4 demonstrate null steering and tapering. In contrast to RF/analog time delay arrays which require additional variable gain amplifiers for adaptive beamforming, the high-resolution CWM with 10-bit coefficients facilitates adaptive null steering and tapering without additional circuitry. Beam 3 is programmed to have a main beam at -30° and a null at 20° while beam 4 has tapered coefficients to suppress sidelobes to less than -25 dB.

Fig. 7(a) compares the power spectral density of a single element to that of the entire array. The measured SNR, SNDR and SFDR for the 16-element array are 60 dB, 60 dB and 71 dB, respectively. Array SNDR, SFDR improve by 11 dB, 14 dB, respectively, compared to a single element. Connecting directly to an antenna without an RF frontend, the measured NF for a single element is 26 dB. The measured EVM is less than -37 dB and no bit errors are observed in 8000 symbols for 5 MBd 256-QAM and 512-QAM (Fig. 7(b)).

Fig. 8 shows measured 16-QAM and 64-QAM constellation diagrams in the presence of an in-band large interferer at a null. Although the power of the interference is 12 dB higher than the desired QAM signal, measured EVM is better than -20 dB for 64-QAM (-24 dB for 16-QAM) and no error symbols are found in 8000 symbols.

Finally, Table I summarizes the performance of the first digital true time delay beamformer IC and compares it with state-of-the-art DBF ICs. The digital beamforming receiver supports 16 elements and generates four independent simultaneous beams with 100 MHz bandwidth and consumes 28 mW per element.

TABLE I
Performance Summary and Comparison

	This Work	[1]	[2]
# of Elements	16	16	8
# of Beams	4	4	2
Delay Implementation	True Time Delay	Phase-Shifting	Phase-Shifting
Bandwidth [MHz]	100	100	20
Array SNDR [dB]	60	59	63
Time Delay Range [ps]	0 - 7500	-	-
ADC Power [mW]	16	15	13
DBF Power [mW]	196	68	19
Total Power [mW]	453	312	124
Active Area [mm^2]	0.29	0.22	0.28
Phase-shifter Resolution [bit]	10	6	10
Technology	40 nm CMOS	40 nm CMOS	65 nm CMOS

V. Conclusion

The work tackles the challenges of squinting and distortion which hinder the implementation of very large beam forming arrays. Phase shifting and time delay are combined to enable the first single-chip true time delay digital beamformer. A new feedback DAC technique reduces distortion in the ADC so that a large array can better benefit from the array SNR gain.

The prototype beamforming receiver achieves near-ideal conventional and adaptive beam patterns which is challenging for analog/RF beamformers. The prototype 4-beam digital beamformer including the 16 CTPBDMs occupies only 0.29 mm^2 and consumes 453 mW.

Acknowledgments

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