# A 2.5 mW 80 dB DR 36 dB SNDR 22 MS/s Logarithmic Pipeline ADC

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***Abstract*—A switched-capacitor logarithmic pipeline analog-to-digital converter (ADC) that does not require squaring or any other complex analog function is presented. This approach is attractive where a high dynamic range (DR), but not a high peak SNDR, is required. A prototype signed, 8-bit 1.5 bit-per-stage logarithmic pipeline ADC is designed and fabricated in 0.18 $\mu$m CMOS. The 22 MS/s ADC achieves a measured DR of 80 dB and a measured SNDR of 36 dB, occupies 0.56 mm$^2$, and consumes 2.54 mW from a 1.62 V supply. The measured dynamic range figure of merit is 174 dB.**

***Index Terms*—Compander, logarithmic ADC, pipeline ADC.**

## I. Introduction

MOST natural signals, including light intensity and audio amplitude, are measured on a logarithmic scale. A properly designed logarithmic coding scheme is more efficient than conventional linear encoding, in that, a higher dynamic range can be represented for a given word length. In a conventional linear analog-to-digital converter (ADC), code-width is uniform over the entire input range. Logarithmic ADCs allow progressively larger quantization errors for larger input values. As an example, since the ability of the human ear to distinguish between different sound levels is less that for larger signal levels, audio signals are well suited to log encoding. Fig. 1 shows that logarithmic coding achieves better image quality than linear coding for the same number of bits.

Expansion of dynamic range is traditionally achieved through an automatic gain control (AGC) amplifier or nonlinear compression [2]. However, an AGC cannot respond to rapidly fluctuating signals. A logarithmic amplifier can be used to compress the dynamic range of an input signal [3], but this approach requires a look-up table to precisely describe the device-derived nonlinear characteristics. Alternatively, a back-end digital compander [4] can be combined with a high-resolution ADC. However, this method is power-hungry and complex. Direct logarithmic analog-to-digital conversion has exactly the same beneficial characteristics as the combination of a logarithmic amplifier and linear ADC, but with potentially much lower power consumption. A direct log adaptation of a conventional linear pipeline ADC replaces subtraction with division, and multiplication by 2 with squaring. Reference scaling [5] enables a log domain pipeline ADC to be implemented with simple scalar multiplication and without cumbersome analog math operations such as squaring or exponents.

In this paper, we describe a logarithmic pipeline ADC technique and present a prototype logarithmic ADC which demonstrates a high dynamic range of 80dB. This approach is advantageous for many applications such as audio, imaging and sensing, where high dynamic range is required. A novel switched capacitor (SC) logarithmic pipeline ADC architecture, that does not require squaring or any other complex analog function, is introduced in Section II. Unlike a conventional pipeline ADC, the pipeline stages do not include an MDAC, so that the required accuracy of the reference voltage is greatly relaxed. Performance metrics such as signal-to-noise-ratio (SNR) and dynamic range are also discussed. Section III highlights the realization of the pipeline architecture and presents circuit details. Finally, the measured performance of a fabricated prototype is presented in Section IV.

## II. Logarithmic Pipeline Architecture

### A. Logarithmic Conversion

With logarithmic coding, the LSB size varies with the input signal level. Similar to a companding digitizer, small signals are quantized at fine resolution, whereas changes in large signals are quantized at coarse resolution. Fig. 2 shows an example of a 5 bit logarithmic companding characteristic. Larger voltage inputs experience coarser quantization.

An L-bit logarithmic ADC converts an input analog voltage ($V_{\rm in}$) to a digital bit sequence $(b_{L-1}, b_{L-2}, \ldots, b_1, b_0)$, mapping to a logarithmic domain. This mapping equation is shown in (1):

$$\log_{10}\left(\frac{V_{\rm in}}{V_{\rm range}} \times 10^{C}\right) = \frac{b_{L-1}2^{L-1} + \cdots + b_0}{2^L} C. \quad (1)$$

In (1), the input voltage $V_{\rm in}$ is divided by the full-scale ADC input range ($V_{\rm range}$), mapping the input to a nominal range from 0 to 1. A *code efficiency* factor, $C$ is introduced. Larger values of $C$ result in a more logarithmic input-to-digital-output relationship, emphasizing smaller signals, and resulting in a higher dynamic range. Fig. 3 illustrates how the code efficiency factor, $C$, affects the input-to-output relationship. Although the LSB size in a conventional ADC, $V_{\rm range}/2^L$, is constant over the entire input range, the normalized logarithmic LSB size of a log-

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Fig. 1. Image quality comparison between 3 bit linear and 3 bit logarithmic coding. (a) Linear 3 bit coding. (b) Log 3 bit coding.

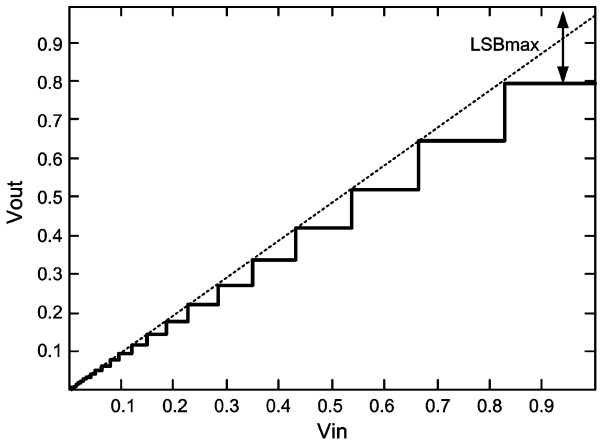



Fig. 2. Companding characteristics of 5 bit logarithmic quantization.

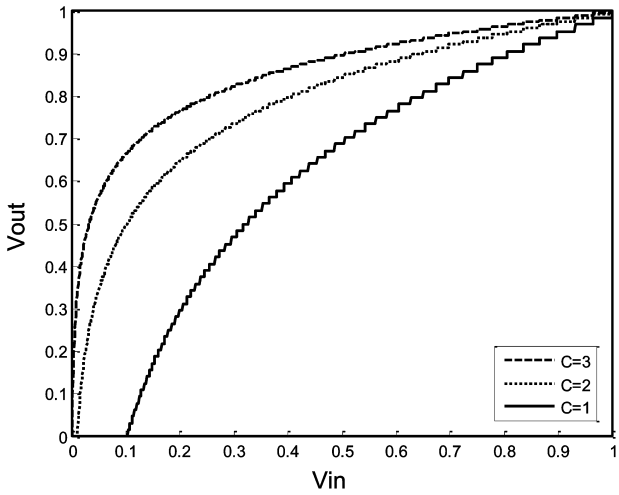



Fig. 3. 6 bit logarithmic characteristics for three values of code efficiencies, $C$.

arithmic ADC is $C/2^{L-1}$, assuming the MSB is used as a sign bit. As a result, the LSB size varies depending on the input amplitude. For the 8 bit logarithmic ADC, which is demonstrated in this work, $C$ is set to 3, resulting in the minimum LSB size to $1.109 \times 10^{-4}$ $\mathrm{V_{range}}$. The theoretical dynamic range, considering only the positive polarity part of the logarithmic ADC range, is 85 dB. A sign bit adds an extra 6 dB, resulting in a theoretical dynamic range of 91 dB. The methodology for calculating theoretical dynamic range is presented later in this section.

Limitations due to noise, linearity, and device matching problems make practical circuit implementations with $C > 3$ difficult. For example, with $C = 2$, and assuming $V_{\mathrm{range}}$ is 1 V, the minimum LSB size of 8 bit ADC is 0.37 mV. On the other hand, with a code efficiency factor of $4(C = 4)$, the minimum LSB size is only 7.5 $\mu$V, which makes noise and matching difficult and impractical to overcome.

By rewriting (1), the analog input corresponding to a digital code is given by

$$\begin{aligned} \nu_{\mathrm{in}} &= V_{\mathrm{range}} \cdot 10^{C\cdot \text{Digital code}/2^L - C} \\ &= V_{\mathrm{range}} \cdot 10^{C\cdot b_{L-1}2^{L-1}+\cdots+b_0/2^L - C}. \end{aligned} \tag{2}$$

The varying LSB size is calculated by subtracting $\nu_{\mathrm{in}}$ values from (2) for two adjacent digital codes. Subtracting analog input values for codes 0 and 1, results in the minimum LSB size. If we subtract the analog input values corresponding to the maximum digital codes $2^L$ and $2^L - 1$, we obtain the maximum LSB size. Equation (3) includes the minimum LSB size and (4) includes the maximum LSB size.

$$\mathrm{LSB_{min}} = V_{\mathrm{range}} \times \left(10^{C/2^L - C} - 10^{-C}\right) \tag{3}$$

$$\mathrm{LSB_{max}} = V_{\mathrm{range}} \times \left(1 - 10^{-C/2^L}\right). \tag{4}$$

The dynamic range (DR) is defined as the ratio of the input range $(V_{\mathrm{range}})$ to the smallest resolvable signal, or the smallest difference between adjacent codes, as

$$\mathrm{DR} = \frac{V_{\mathrm{range}}}{\min(V_{\mathrm{trip},j+1} - V_{\mathrm{trip},j})} = \frac{V_{\mathrm{range}}}{\mathrm{LSB_{min}}}. \tag{5}$$

Then, by substituting (3), dynamic range is calculated as

$$\begin{aligned} \mathrm{DR} &= 20\log_{10}\frac{V_{\mathrm{range}}}{\mathrm{LSB_{min}}} \\ &= -20\log_{10}\left(10^{C/2^L - c} - 10^{-c}\right)_{(\mathrm{dB})}. \end{aligned} \tag{6}$$

### B. Logarithmic Pipeline ADC Architecture

This logarithmic ADC architecture is fundamentally different to the classical linear pipeline architecture. A linear one-bit-per-

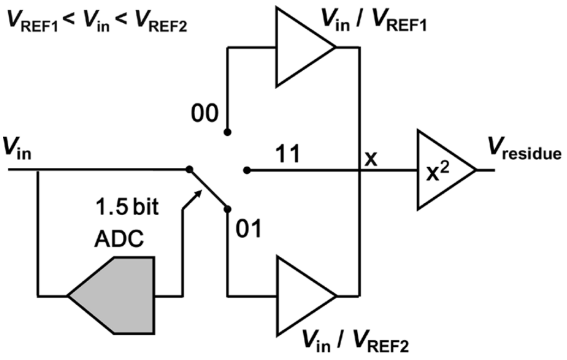



Fig. 4. Possible implementation of logarithmic pipeline ADC stage.

stage pipeline ADC subtracts binary-weighted values of the reference from the input, attempting to reach a final residue of zero at the end of the pipeline. On the other hand, this logarithmic pipeline architecture gains up the input to each stage, attempting to ultimately achieve a residue of full-scale at the end of the pipeline.

The proposed logarithmic-domain pipeline ADC architecture is based on simple scalar multiplication and does not require cumbersome analog math operations such as squaring or exponents. A direct log-adaptation of a conventional linear 1.5-bit-per-stage, pipeline ADC would replace subtraction with division, and multiplication-by-2 with squaring. Since $\log_{10} V_{\rm in} - \log_{10} V_{\rm ref} = \log_{10}(V_{\rm in}/V_{\rm ref})$, in a logarithmic pipeline ADC a conditional attenuation (or gain) replaces subtraction, depending on the decision of the sub-ADC. This log pipeline stage differs from a conventional 1.5 bit linear pipeline ADC stage, which subtracts one of three possible MDAC outputs. In the conventional linear 1.5 bit-per-stage pipeline ADC, the stage input signal is quantized by a 1.5 bit sub-ADC and the analog residue is multiplied by 2 to fit the full-scale input range of next stage. Instead, the logarithmic 1.5 bit-per-stage architecture sets one of three different inter-stage gains depending on the sub-ADC decision. These three gain settings are achieved by switching in different values of feedback capacitance across an opamp. Fig. 4 shows a possible implementation of a stage in a logarithmic 1.5-bit-per-stage ADC.

Although Fig. 4 also includes a squarer, we next see how squaring is eliminated in this log ADC architecture. Squaring in a log ADC is equivalent to a multiplication by 2 in a linear radix-2 pipeline ADC. Considering that $2 \times \log_{10}(V_{\rm residue}) = \log_{10}(V_{\rm residue}^2)$, this requires squaring of the residue, but accurate and reliable squaring is difficult in the analog domain. Instead of attempting precise analog squaring, we achieve the same overall result by scaling the comparator reference voltages and gain settings for each pipeline stage. (A similar scheme is proposed in [6].)

Fig. 5(b) shows the residue characteristic of a 1.5 bit logarithmic ADC pipeline stage. For comparison, a direct linear relationship between input and output is plotted in Fig. 5(a). The residue plots are on a logarithmic sale with a normalized $\log_{10}$ range from $-3$ to 0 (i.e., $C = 3$). The residue of Fig. 5(b) is

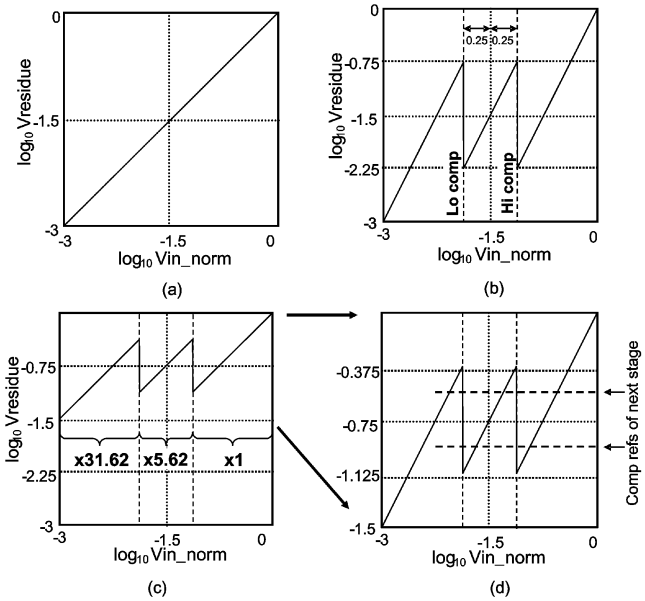



Fig. 5. Logarithmic ADC residue plot. (a) Gain of 1 over log input range. (b) Desired 1.5 bit residue but squaring is difficult. (c) Conditional multiplication — no squaring. (d) Rescale refs to get desired characteristic.

divided into three regions as there are two comparators. A modified approach in Fig. 5(c) uses the same comparator thresholds, but the gain settings are chosen so that the residue now falls entirely into the top vertical half (i.e., logarithmic range: $-1.5$ to 0, or a corresponding linear range: $10^{-1.5}$ to 1). Squaring of the residue of Fig. 5(c) would double its logarithmic range to appear identical to the residue of 5(b). However, instead of squaring, a different set of comparator reference voltages is chosen for the next stage. The reference voltages are set in the top half of 5(c), effectively achieving a rescaled residue with the same shape (Fig. 5(d)). This approach is not only easier to implement but also advantageous since the reference and signal voltages become larger (i.e., closer to a normalized logarithmic value of 0) going down the pipeline. For example, the upper threshold of the second stage is 137 mV, whereas that of the first stage is 31.6 mV. Larger references are easier to generate and allow more tolerance for comparator errors.

The classic 1.5 bit-per-stage redundancy scheme used in linear pipeline ADCs [7] is adapted here to reduce the required accuracy of the comparators. Unlike the case with a linear pipeline, reference voltages are not used in MDAC stages, and therefore, redundancy significantly reduces the required accuracy of both the comparators and the voltage references. In a 1.5 bit stage, the input range of each stage is divided into three regions, corresponding to the three possible outputs of the two comparators: "00", "01" and "11". Redundancy can correct for both comparator offset errors and reference voltage errors with a range given by

$$\Delta V_{\rm in,correct} = \log_{10} V_{\rm ref} \pm \left(\frac{1}{4}\right) \log_{10} V_{\rm ref}. \qquad (7)$$

The easiest way to calculate the reference voltages is to begin on a logarithmic scale and then to return to linear scale. In the residue plot for the $i$th stage, the midvalue of the $x$ axis is at

TABLE I
VOLTAGE REFERENCE AND GAIN SETTINGS IN PROTOTYPE 8 BIT ADC ($C = 3$)

| Stage ($i$) | 1st | 2nd | 3rd | 4th | 5th | 6th |
|---|---|---|---|---|---|---|
| $V_{ref1i}$ | 6.7 $mV$ | 57.7 $mV$ | 169.9 $mV$ | 291.5 $mV$ | 381.8 $mV$ | 0.417 $V$ |
| $V_{ref2i}$ | 37.5 $mV$ | 136.9 $mV$ | 261.6 $mV$ | 361.7 $mV$ | 420.3 $mV$ | 0.449 $V$ |
| $G_{1i}$ | 31.62 | 5.62 | 2.37 | 1.53 | 1.24 | 1.16 |
| $G_{2i}$ | 5.62 | 2.37 | 1.53 | 1.24 | 1.11 | 1.08 |
| $G_{3i}$ | 1 | 1 | 1 | 1 | 1 | 1 |

$-C/2^i$ on a logarithmic scale. If digital correction is applied, then from (7) reference voltages are defined as

$$\log_{10}\frac{V_{\text{ref1}i}}{V_{\text{range}}} = -\frac{C}{2^i}\left(1 \pm \frac{1}{4}\right)$$
$$V_{\text{ref1}i} = V_{\text{range}} \times 10^{-1.25C/2^i}$$
$$V_{\text{ref2}i} = V_{\text{range}} \times 10^{-0.75C/2^i} \tag{8}$$

where $Vref_{1i}$ is the lower threshold and $Vref_{2i}$ is the upper threshold. Similarly, the gains for stage $i$ are

$$\log_{10} G_{1i} = \frac{C}{2^i}, \quad \log_{10} G_{2i} = \frac{C}{2\cdot 2^i}, \quad \log_{10} G_{3i} = 0$$
$$G_i(\nu_{\text{in}}) = \begin{cases} G_{1i} = 10^{C/2^i}, & \nu_{\text{in}} \le V_{\text{ref1}i} \\ G_{2i} = 10^{C/2^{i+1}}, & V_{\text{ref1}i} < V_{\text{in}} \le V_{\text{ref2}i} \\ G_{3i} = 1, & V_{\text{ref2}i} < \nu_{\text{in}} \le V_{\text{range}}. \end{cases} \tag{9}$$

In (9), $G_{1i}$ is the highest gain setting for stage inputs less than $V\text{ref}_{1i}$; $G_{2i}$ is the midrange gain for the stage inputs that lie between $V\text{ref}_{1i}$ and $V\text{ref}_{2i}$; and $G_{3i}$ is the bypass gain for the stage inputs larger than $V\text{ref}_{2i}$ for the $i$th stage. Note that $G_{1i} = G_{2i}^2$. Table I gives the stage reference and gain settings in the prototype 8 bit ADC designed with $C = 3$.

### C. Gain Error in the Logarithmic Pipeline ADC

In a conventional pipeline ADC, gain errors are caused by capacitor mismatch, by finite opamp gain, and by incomplete settling of the residue amplifiers. These gain errors reduce the linearity of the ADC. While both MDAC errors and gain errors are sources of nonlinearity in a conventional pipeline ADC, only gain errors contribute to nonlinearity in this logarithmic pipeline structure because it does not include an MDAC.

Ideally, a stage output is the product of the input signal and the gain; $\nu_{\text{out}} = \nu_{\text{in}} G(\nu_{\text{in}})$, where $G(\nu_{\text{in}})$ is the ideal closed-loop gain of the inter-stage amplifier defined in (9). If we express the total gain error as $\varepsilon(\nu_{\text{in}})$, then the actual gain is $G(\nu_{\text{in}})(1 + \varepsilon(\nu_{\text{in}}))$. For example, without gain error, the midrange gain of the first stage of the prototype ADC is 5.62, but varies from 5.57 and 5.68 with a $\pm 1\%$ capacitor matching error. If we express the relationship between the input and output of each pipeline stage in the logarithmic domain, the stage output or residue can be written as

$$\log_{10}\nu_{\text{out}} = \log_{10}\nu_{\text{in}} + \log_{10} G(\nu_{\text{in}}) + \log_{10}(1+\varepsilon(\nu_{\text{in}})). \tag{10}$$

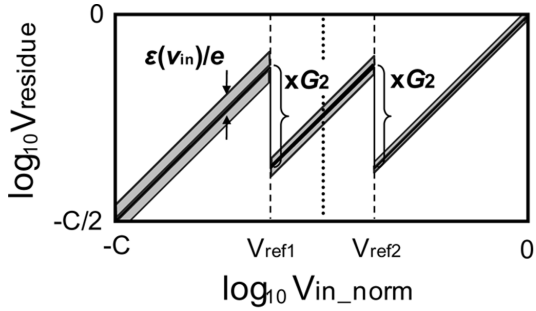



Fig. 6. 1.5 bit residue plot and error due to finite gain.

If $\varepsilon$ is small ($|\varepsilon(v_{\text{in}})| \ll 1$), we can approximate $\log_{10}(1 + \varepsilon(\nu_{\text{in}})) \approx \varepsilon(\nu_{\text{in}})/e$, where $e$ is the natural logarithmic constant ($e \approx 2.718$) giving

$$\log_{10}\nu_{\text{out}} = \frac{\log_{10}\nu_{\text{in}} + \log_{10} G(\nu_{\text{in}}) + \varepsilon(\nu_{\text{in}})}{e}. \tag{11}$$

A new residue plot considering gain error is drawn in Fig. 6. The last term in this equation, $\varepsilon(\nu_{\text{in}})/e$, causes an undesired gain shift of $\varepsilon(\nu_{\text{in}})/e$ in logarithmic domain. The $\varepsilon(\nu_{\text{in}})/e$ term represents the input referred error in the logarithmic relationship between the stage input and output.

The gain error, $\varepsilon(\nu_{\text{in}})$, can be divided into a random component and a systematic component; $\varepsilon(\nu_{\text{in}}) = \varepsilon_r + \varepsilon_f(\nu_{\text{in}})$. The random part, $\varepsilon_r$, is due to device imperfections, in particular capacitor mismatch. Since different capacitors are used for each of the three gain settings, capacitor mismatch can cause INL errors. For example, a 1% capacitor mismatch in one of the gain settings of the first stage, results in an INL error of 0.16 LSB. (Note that in a signed 8 bit logarithmic ADC with $C = 3$, an $\text{LSB} = C/2^{L-1} = 0.023$ in logarithmic domain.) The systematic component, $\varepsilon_f(\nu_{\text{in}})$, results from deficient amplifier gain and is inversely proportional to the feedback factor ($\beta$). In other words, the systematic component of gain error is predictable if we know the feedback factor and the opamp gain.

The systematic gain error can be derived from finite DC gain as

$$\varepsilon_f(\nu_{\text{in}}) = \frac{1}{G(\nu_{\text{in}})}\cdot\frac{A_0}{1+\beta A_0} - 1$$
$$= -\frac{G(\nu_{\text{in}})}{G(\nu_{\text{in}}) + A_0} \approx -\frac{G(\nu_{\text{in}})}{A_0} \tag{12}$$

where $A_0$ is the opamp gain, and we assume that $\beta$, the feedback factor is the inverse of $G(\nu_{\text{in}})$, the ideal gain. Using this approximation for gain error, Fig. 7 plots the systematic component of the closed-loop stage gain error due to finite DC gain. The gain error depends on the gain setting, and therefore there is a different gain error for each of the three input regions defined in (9). The absolute value of gain error in the low-range is $G_2$ times larger than that in the midrange, since according to (9) $G_1$ is the square of $G_2$.

Referring to (10), we see that a constant value of $\varepsilon_f$ causes an offset in the log relationship between stage input and output. The grey *common offset* line in Fig. 7 set at $-(G_1+1)/(2eA_0)$ represents the average of the maximum gain error (occurs in the low range) and the minimum gain error (occurs in the high

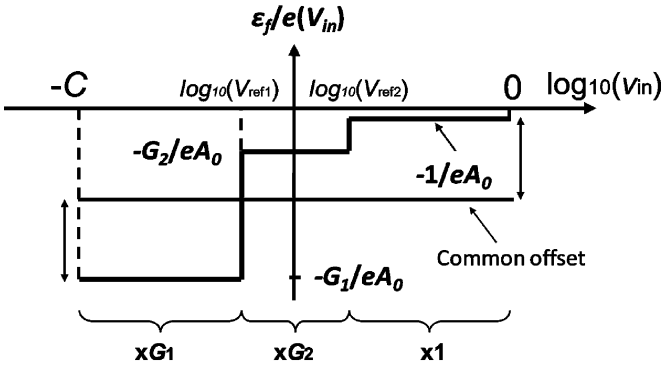



Fig. 7. Input-referred systematic stage gain error due to finite opamp gain for a 1.5-bit logarithmic stage.

range). The effective integral nonlinearity is the maximum distance from $\varepsilon_f(\nu_{\rm in})/e$ to the average (i.e., to $(G_1-1)/(2eA_0)$).

To guarantee the overall ADC linearity, the effective systematic error should be less than the LSB size. To achieve an INL less than 0.5 LSB, the maximum stage gain error of the first stage can be up to 3.1%, compared to only 0.62% [9] in an 8 bit linear ADC. Unlike a linear ADC the logarithmic ADC does not include an MDAC, further relaxing the requirements for linearity. In practice, in a conventional linear ADC, the nonlinearity error caused by MDAC is larger than the nonlinearity caused by gain error [9].

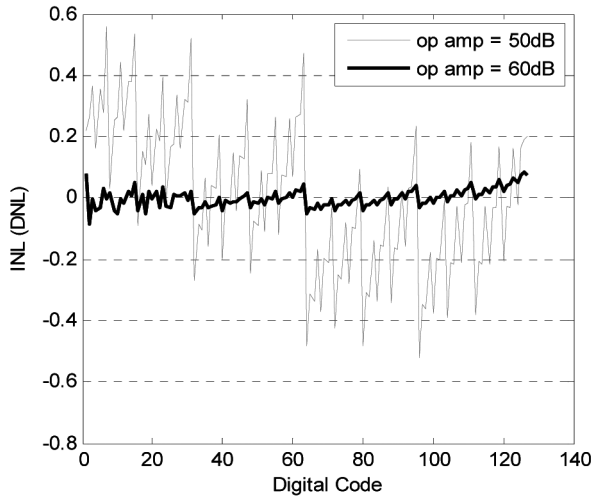
From the above, we can also estimate the minimum gain required for the opamp

$$\frac{G_1-1}{2eA_0} < \text{LSB} \Rightarrow A_0 > \frac{G_1-1}{2e}\cdot\frac{1}{\text{LSB}} = \frac{10^{C/2i}-1}{2e}\cdot\frac{2^{L-1}}{C} \tag{13}$$

where $C$ is the code efficiency factor. As shown in (13), the gain requirement decreases exponentially down the pipeline. To achieve an INL less than 1 LSB, the minimum opamp gain of the first stage should be greater than $240.3$ $(= 47.6$ dB$)$, but only $36.3$ $(= 31.2$ dB$)$ in the second stage. This theory was tested with a behavioral model, which considers both finite op amp gain and capacitor mismatch. Fig. 8(a) shows an INL plot for opamp gains of 50 dB and 60 dB INL. Fig. 8(b) shows a histogram of worst INL for a 1000 sample Monte Carlo simulation, which assumes with a $1\sigma$ capacitance error of 1% for a 0.1 pF unit capacitor. From the behavioral simulations, we see that the logarithmic scheme has immunity to both gain error and capacitor mismatch as we discuss in this section. In addition, the input-referred offsets in pipeline stages are code-dependent and affect the linearity performance. The offsets are modeled in the behavioral simulation and the offset requirements per stage that guarantees less than 1 LSB of the INL are shown in Table II.

## III. Logarithmic Pipeline ADC Prototype Implementation

A signed 8-bit, 6-stage, fully differential, logarithmic pipeline converter is implemented as shown in Fig. 9. The gain and references values, shown in the figure are derived using (8) and (9) with $C = 3$. Much like a linear pipeline ADC, each stage includes a 1.5 bit sub-ADC. However, instead of a 3-level MDAC,



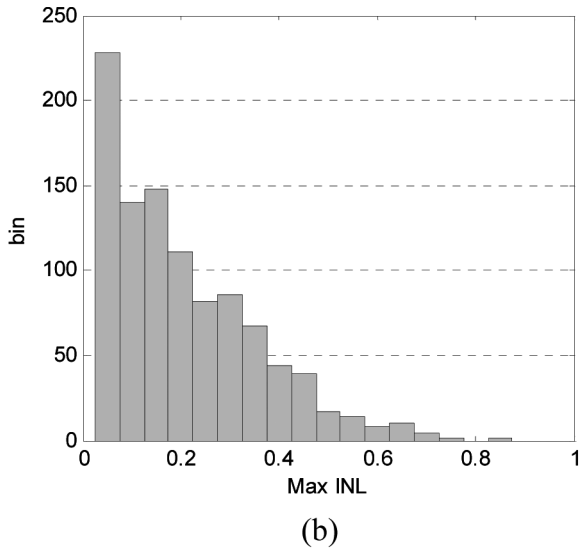




Fig. 8. Linearity test from a behavioral model. (a) INL plot for finite op amp gain. (b) Worst case INL histogram for Monte Carlo simulation with mismatched capacitors.

TABLE II
Input-Referred Offset Requirements in Prototype 8 bit ADC ($C = 3$)

| Stage ($i$) | 1st | 2nd | 3rd | 4th | 5th | 6th |
|---|---|---|---|---|---|---|
| $V_{offset}$ | 3.2 $mV$ | 6.5 $mV$ | 13.1 $mV$ | 26 $mV$ | 53 $mV$ | 105 $mV$ |

one of three gain settings is selected by switching in different values of feedback capacitor across an operational amplifier, depending on the sub-ADC decision. As discussed above, the redundant 1.5b architecture relaxes the requirements for comparator accuracy and comparator reference voltage accuracy. The accuracy of a stage residue is largely unaffected by errors or noise on a distributed reference since the residue is decided by a programmable gain and not MDAC subtraction.

Fig. 10 shows a fully differential pipeline stage controlled by two non-overlapping $\Phi 1$ and $\Phi 2$. One of three feedback capacitors is selected to give one of three different gains depending on

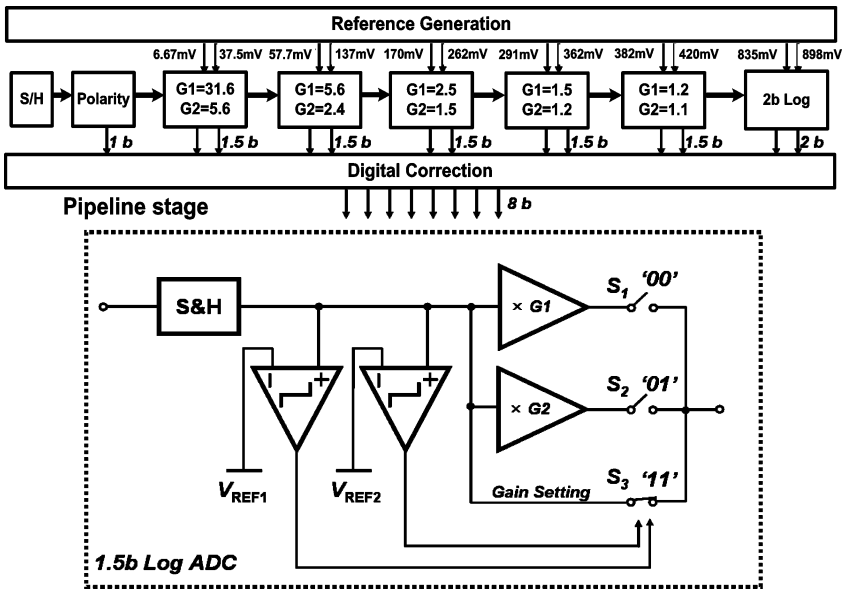



Fig. 9. Logarithmic ADC architecture.

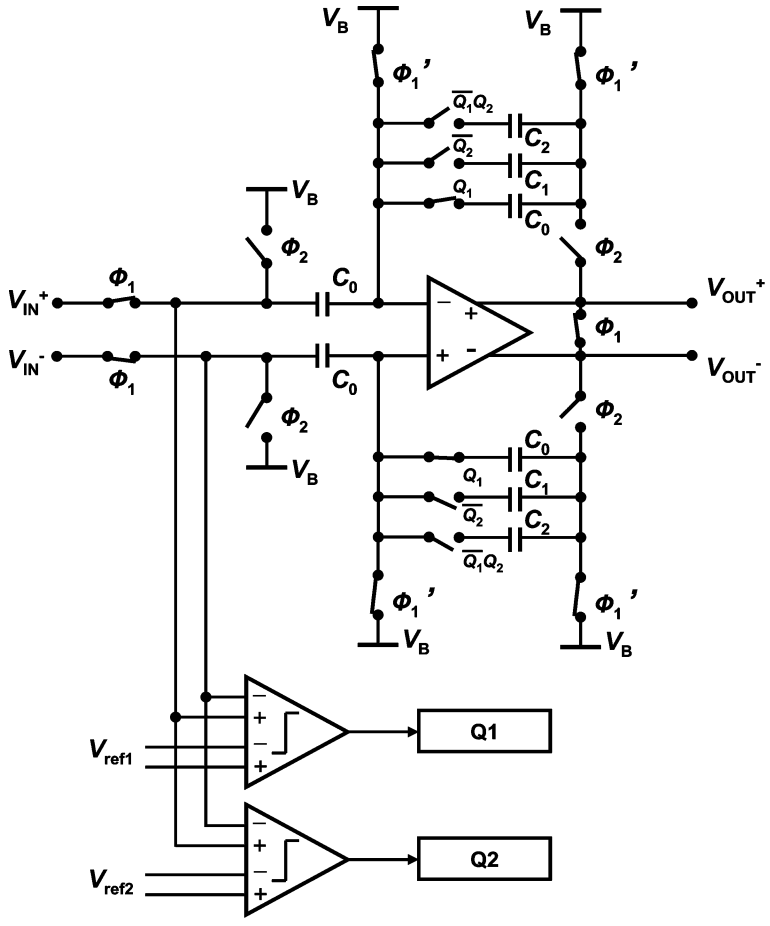



Fig. 10. Logarithmic ADC stage.

the sub-ADC decision. While $\Phi 1$ is high, the stage input is sampled, and the feedback capacitor is reset. $\Phi 2$ is the gain phase.

Since this logarithmic stage does not use an MDAC, the reference voltage settling requirement is relaxed in this architecture. The common mode bias, $V_B$, is only used to reset the common mode voltage which is 600 mV in the prototype. The operational amplifiers are implemented as folded cascode amplifiers with pMOS input pairs. A common mode feedback circuit maintains the common mode output voltage at 600 mV. Since large signals are more coarsely quantized than small signals in logarithmic conversion, the logarithmic ADC is less sensitive to opamp gain nonlinearity.

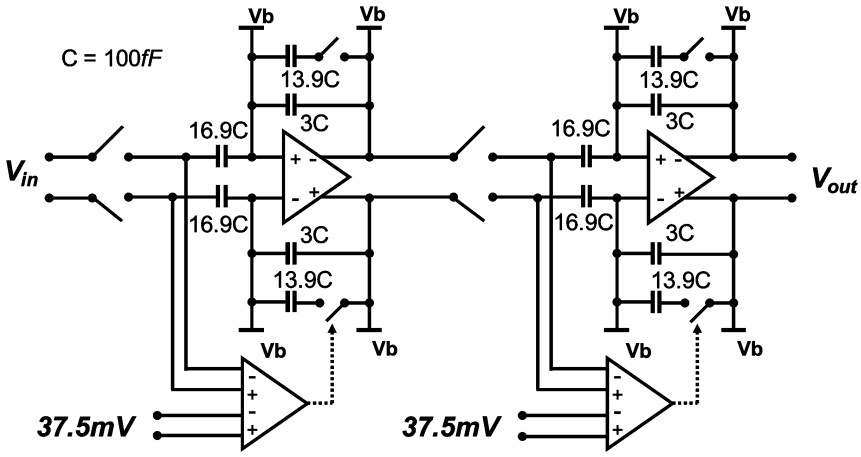



Fig. 11. The first pipeline stage is comprised of a cascade of two SC amplifiers.

Since the highest gain setting for the first stage is 31.6 (the gain settings are 31.6, 5.6 and 1) a cascade of two programmable SC gain stages is used to implement the first pipeline stage, as shown in Fig. 11. One of the two comparators for the first stage is placed in front of each amplifier. The amplification of the first SC gain stage allows the same reference voltage to be used for both comparators and also relaxes the accuracy required for lower reference voltage. Subsequent pipeline stages require far less gain and are implemented with single SC amplifiers. Capacitors are implemented as multiples of a unit capacitor (100 fF). The use of unit ratios causes a slight error in stage gain, for example, a capacitor ratio of $17/3 = 5.66$ differs from the ideal gain of 5.62 for the first stage by 0.7%. However, this 0.7% gain error is well tolerated by the architecture, and the use of unit capacitors improves capacitor matching. Since a large input-referred offset affects the linearity of the ADC, transistor matching was carefully considered especially for the first stage. Common-centroid multi-fingered layout is used for the critical transistors. The sixth stage of the pipeline is a 2-bit logarithmic flash ADC. All stage reference voltages are generated on-chip as shown in Fig. 12.

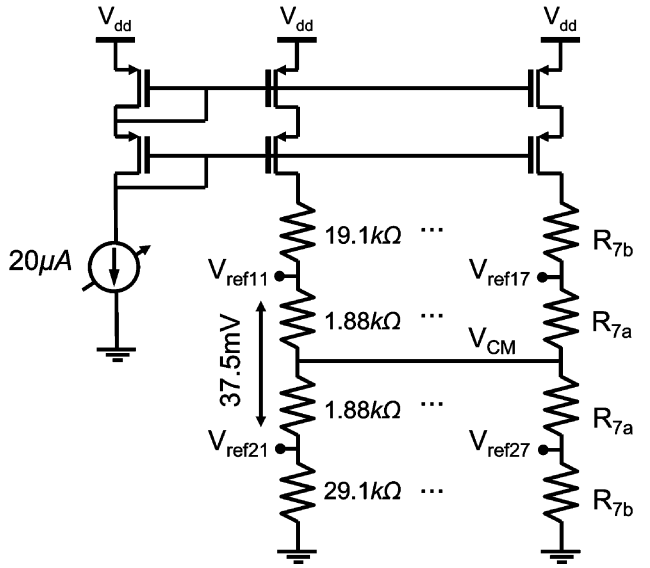



Fig. 12. Reference voltage generation.

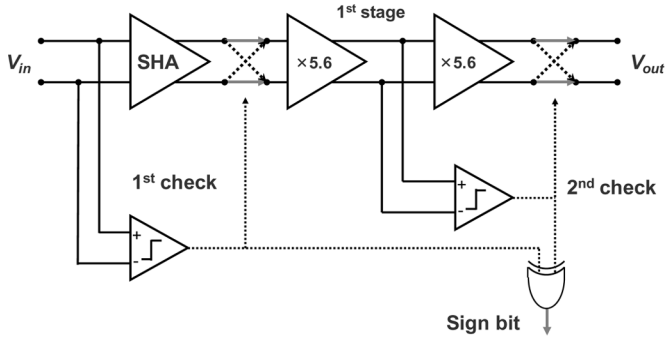



Fig. 13. Polarity decision scheme.

A logarithmic function is not defined for negative inputs, but most differential natural signals have a polarity [11]. To handle negative signals, a first sign decision is made at the front of the pipeline as shown in Fig. 13. The sign stage determines the input polarity, and if necessary inverts the polarity of input to the remainder of the pipeline. This sign decision must ultimately be made at the full accuracy of the ADC. To achieve the required accuracy, the sign decision is made by a combination of two comparators; one after the front-end SHA and another at the output of the first stage. The second comparison is much more accurate because of the gain of the first stage. The estimate made at the input of the front-end comparator is sufficiently accurate to allow the first stage to correctly process the input. For small inputs where the ADC is more sensitive to sign errors, the first stage is set to the high gain setting of 31.6, with each of the cascaded amplifiers providing a gain of 5.6. In the prototype device, without correction the first decision should be accurate to 222 $\mu$V, however the second decision has a margin of 1.25 mV because this second decision is made after $\times 5.6$ multiplication by the first stage. If the first decision is wrong, the second comparator corrects the polarity. An XOR of the first decision and the second decision generates the sign bit (MSB).

A differential flip-around sample and hold as shown in Fig. 14 is used for fast and linear operation [12]. The operational amplifier used in the sample and hold circuit has the same folded cas-

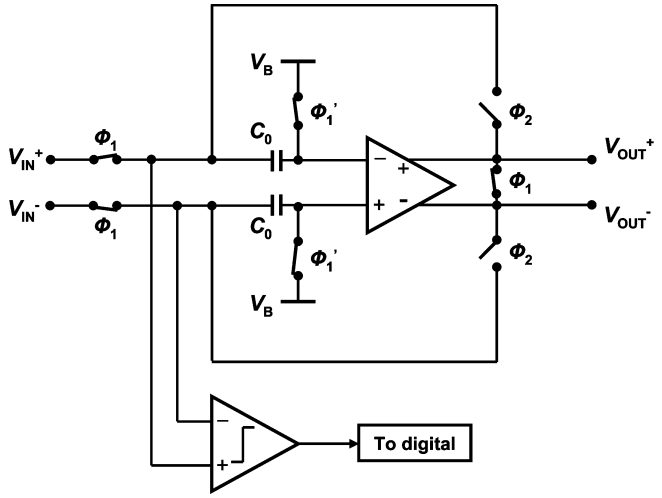



Fig. 14. Sample and hold circuit, and first polarity check comparator.

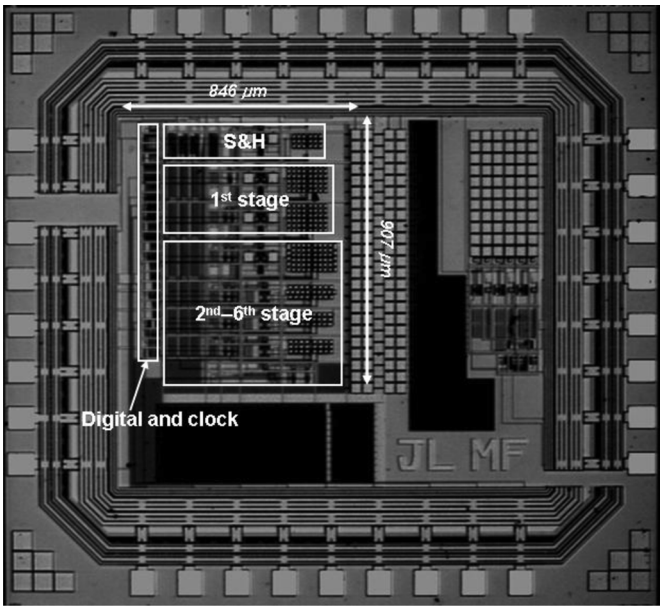



Fig. 15. Logarithmic ADC die micrograph.

coded structure as that of the amplifiers in the pipeline stages. To minimize the effect of charge injection, bottom plate sampling is used [13]. A two-stage regenerative comparator technique based on [14] is employed. D-flip-flops perform synchronization of data from different stages and a ripple carry adder adds the synchronized data to produce the overall 8-bit digital output [15], [16].

## IV. Prototype Measurements

A prototype device is fabricated in 0.18 $\mu$m CMOS with a MiM capacitor option and occupies 0.56 mm$^2$ (2.1 mm$^2$ including I/O) as shown in Fig. 15. The ADC consumes 2.54 mW at 22 MS/s (including clock, reference generation, biasing, and digital circuitry) from a 1.62 V analog supply and a 1.78 V digital supply.

Plots of the DNL and INL values obtained from measurements of the prototype ADC are shown in Fig. 16. The measured

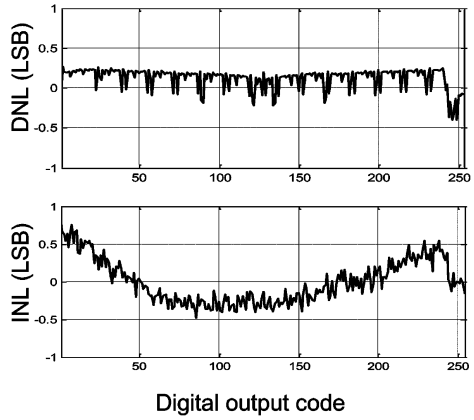



Fig. 16. Measured DNL and INL of logarithmic ADC.

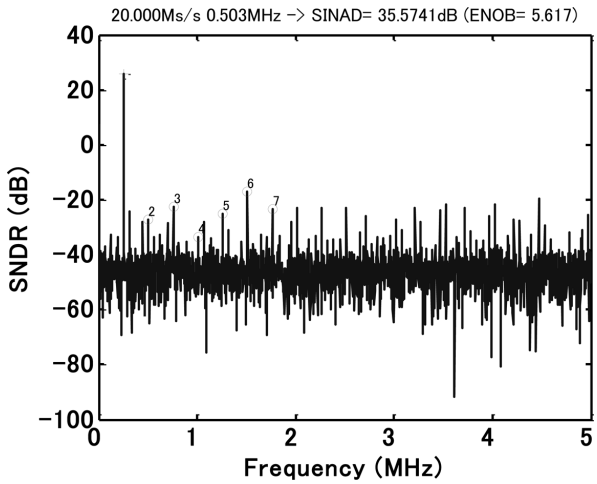



Fig. 17. Spectral density plot with 503 kHz single tone input signal.

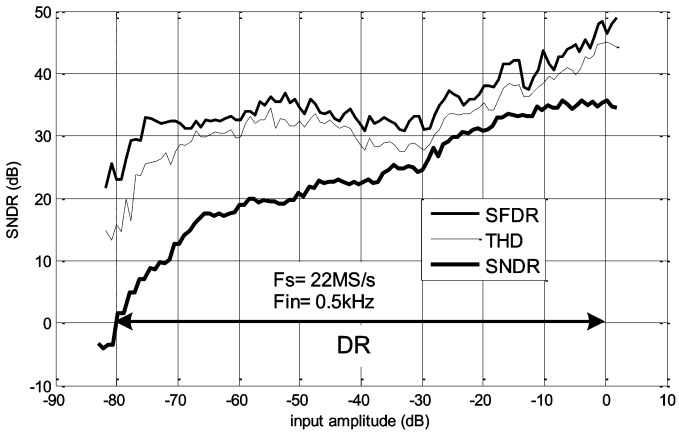



Fig. 18. Measured SNDR, SFDR, and THD versus input amplitude.

maximum $|\mathrm{DNL}|$ and $|\mathrm{INL}|$ are 0.32 LSB and 0.77 LSB, respectively. The DNL curve looks shifted up by 0.2 LSB with peaking in every 16th code step. This seems to be result of the reference mismatch of the 4th stage and the final stage. The average of INL curve is adjusted to zero. The MSB (sign bit) divides the upper half codes and the lower half codes. In the DNL and INL plots, the lower half codes ($0 \sim 127$) are flipped to show code versus input relationship. The definitions of DNL and INL for

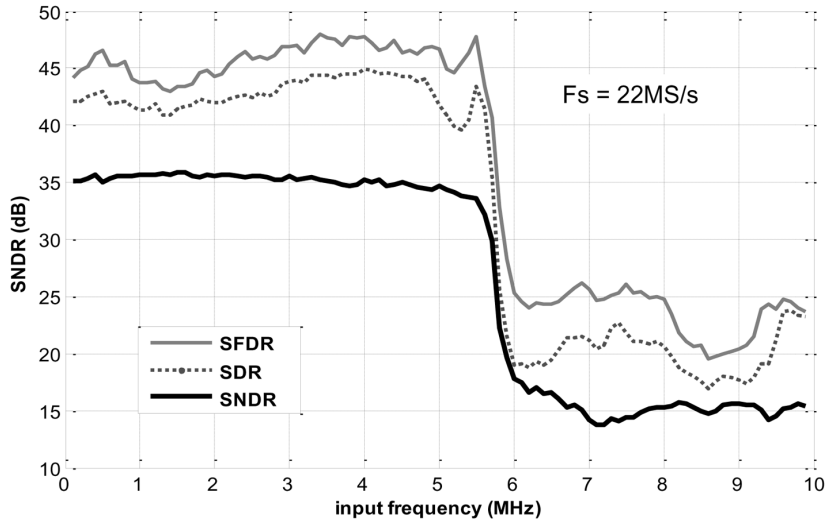



Fig. 19. Measured SNDR, SFDR, and THD versus input frequency.

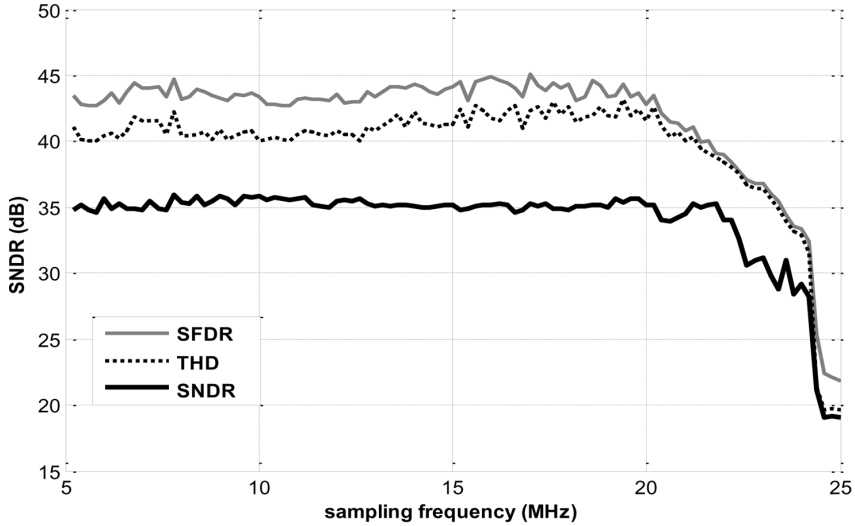



Fig. 20. Measured SNDR, SFDR, and THD versus sampling frequency with 100 kHz input signal.

a logarithmic ADC are similar to those for a linear ADC except that in a logarithmic ADC the ideal step size is different for each code.

$$\mathrm{DNL}(j) = \frac{V_{\mathrm{trip}} - V_{\mathrm{ideal}}}{V_{\mathrm{ideal}}}, \quad \mathrm{INL}(j) = \sum_{i=1}^{j},$$
$$\mathrm{DNL}(i)j \in \{x | x \in N, 1 \leq x \leq 2^L - 2\}. \tag{14}$$

A major difference between a linear ADC and a logarithmic ADC is that, for the latter, the LSB size varies along with the input signal (while the ratio of adjacent trip voltages remains constant). To measure the nonlinearity with a histogram test, we exploit the fact that the code density of a logarithmic ADC follows an exponential function. For a sinusoidal input, each code bin for an ideal logarithmic ADC is calculated through integration of a probability density function as

$$P_{\log}(n) = \frac{1}{\pi}\left[\arcsin(10^{Cn/2^L - C}) - \arcsin(10^{Cn - 1/2^L - C})\right] \tag{15}$$

TABLE III
PERFORMANCE COMPARISON

| | [3] | [17] | [18] | **This Work** |
|---|---|---|---|---|
| Dynamic Range | 60 *dB* | 58.4 *dB* | 77 *dB* | **80.2 *dB*** |
| Topology | log diode | Linear | ∑Δ | **log pipeline** |
| Speed (2x BW*) | 312.5 *S/s* | 30 *MS/s* | 20 *MHz** | **22 *MS/s*** |
| SNDR | 49 *dB* | 58.4 *dB* | 69 *dB* | **35.6 *dB*** |
| Power | 3 $\mu W$ | 4.7 *mW* | 56 *mW* | **2.54 *mW*** |
| $FOM_1$ (*pJ/con.step*) | 40.1 | 0.23 | 0.24 | **2.38** |
| $FOM_2$ (*dB*) | 137.2 | 156.5 | 162.5 | **174** |

where $n$ is the digital code, $C$ is the code efficiency factor and $L$ is the number of bits.

800,000 points were collected at a sampling rate of 22 MS/s of a 503 kHz sinusoid for the code density test of the prototype 8 bit ADC. The code density test with a sinusoidal input signal

has a known limitation in the case of log converters since the probability of hitting a code is very low for codes near zero. To overcome this limitation a large number of points should be collected.

Fig. 18 shows the measured dynamic performance versus input amplitude. The peak measured DR, SFDR and SNDR are 80 dB, 44 dB and 36 dB, respectively. The measured dynamic range is the difference in input level between the minimum detectable signal (i.e., $\mathrm{SNDR} = 0$) and the maximum resolvable signal (at highest-peak SNDR).[1] The dynamic range is far greater than that of a linear ADC, however nonlinear logarithmic conversion somewhat degrades peak SNDR. Nevertheless, the measured peak SNDR is close to the 37.9 dB ideal value for a compression of $C = 3$ implemented in the prototype. Figs. 19 and 20 show the measured dynamic performance versus input frequency and sampling frequency, respectively. During test, a single tone sinusoidal input is applied and the measured digital output is reconstructed according to the ADC's exponential characteristic. As shown in Fig. 19, SNDR falls above 6 MHz. Although the two comparator polarity-detection scheme (Fig. 13) can correct for errors made by the comparator in front of the sample-and-hold, correction may fail for fast-slewing high-speed inputs.

## V. Conclusion

A logarithmic pipeline ADC architecture that does not rely on squaring or device exponential behavior is proposed and implemented. Since the pipeline does not include MDAC, the required accuracy of the reference voltage is relaxed. A prototype logarithmic ADC was fabricated in 0.18 $\mu$m CMOS technology and the measurements of the logarithmic ADC prototype show a high dynamic range, comparable to sigma-delta ADC, but achieved with a wide bandwidth and very low power consumption.

Two figures of merit are compared with recently published converters in Table III.

The figure of merit $(\mathrm{FOM}_1)$ is

$$\mathrm{FOM}_1 = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \times Fs} \frac{J}{\mathrm{conversion-step}} \tag{16}$$

(based on total power consumption including clock, reference generation, biasing, and digital circuitry) is 2.38 pJ/conversion-step. The dynamic range figure of merit $(\mathrm{FOM}_2)$ is 174 dB.

$$\begin{aligned}\mathrm{FOM}_2 &= 20\log_{10}(\mathrm{DR}) + 10\log_{10}(\mathrm{BW}) \\ &\quad - 10\log_{10}(\mathrm{Power}) \\ &= 174\ \mathrm{dB}.\end{aligned} \tag{17}$$

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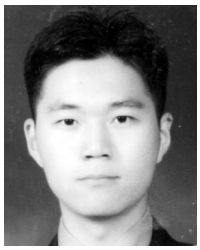
[1] A different definition of dynamic range is required in communication applications where the desired signal must be digitized in the presence of a strong interferer. However, there are many applications, such as audio and video, where the signal does not suffer from blockers and interferers.

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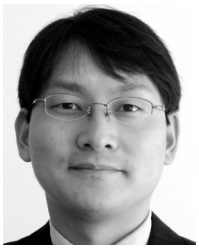

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