

A Reconfigurable FIR Filter Embedded in a 9b Successive Approximation ADC

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Abstract—A reconfigurable FIR filter and 9b SAR ADC combination in 0.13 μm CMOS is presented. The filter does not require additional analog circuitry, but is implemented by using the SAR capacitor array with a modified tracking and sampling scheme. The prototype filter-ADC can be digitally configured as a 4-tap filter, as one of two different 12-tap filters, or without any filtering. The prototype occupies an active area of 0.68mm², achieves 45dB SNDR and dissipates 7.3mW power at 5MS/s. The lowest frequency notch of the embedded filter attenuates by as much as 30.5dB in 4-tap mode and 38.4dB in 12-tap mode.

I. INTRODUCTION

A key bottleneck in the development of the digital radio receiver is the difficulty in implementing integrated, low power, programmable filters. This paper introduces a filtering technique based on modification of sampling in a SAR ADC. The filter can be adapted on the fly to target blockers and interferers by changing its sampling configuration; yet, the filter-ADC combination adds minimally to power consumption, complexity and area when compared to a SAR ADC alone. This filter also supplements the anti-aliasing filter, thus allowing a reduction in ADC conversion rate and/or a reduction in the complexity of DSP or analog filtering. The fabricated prototype can be digitally configured as a 4-tap filter, as one of two different 12-tap filters, or without any filtering.

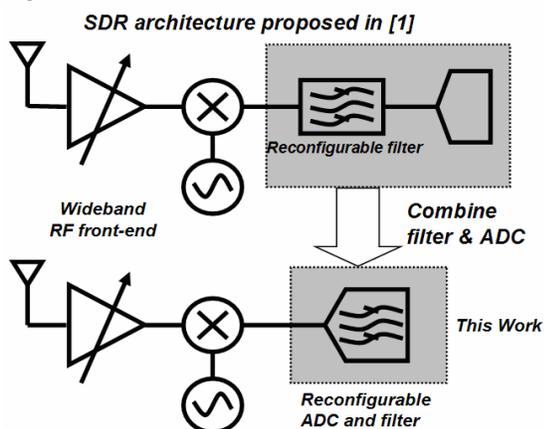


Fig. 1. Proposed reconfigurable digital radio receiver architecture.

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The proposed architecture achieves a higher level of integration when compared to recently demonstrated work on charge-domain filtering based digital radios. This is accomplished by integrating the filter into the ADC sampling process. Such integration can eliminate the explicit filtering stages found in traditional receiver front-ends, as shown in Fig. 1.

The receiver in [1] utilizes discrete-time (DT) current subsampling decimation filters and adjusts sampling rates and capacitor groupings in order to optimize the frequency response for each of 4 different GSM/GPRS bands. The authors of [2] demonstrate a direct conversion receiver for different communication standards by utilizing DT capacitive decimation anti-aliasing filters. The output of both [1] and [2] require resampling by an external ADC. The proposed design achieves DT filtering by modifying capacitive sampling in a SAR ADC and therefore eliminates resampling at the ADC. A key advantage of the proposed filtering technique is that the input signal is sampled only once by the filter-ADC combination, so that noise is not introduced both by DT filter sampling and ADC resampling of the filter output. Assuming that kT/C noise dominates, noise is halved. Furthermore, since there is only one set of capacitors, the total capacitance is reduced by a factor of 4.

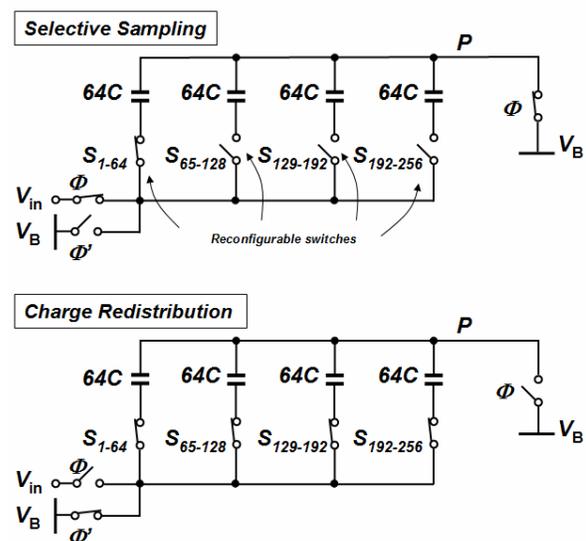


Fig. 2. Principle of filtering with charge sharing sampling.

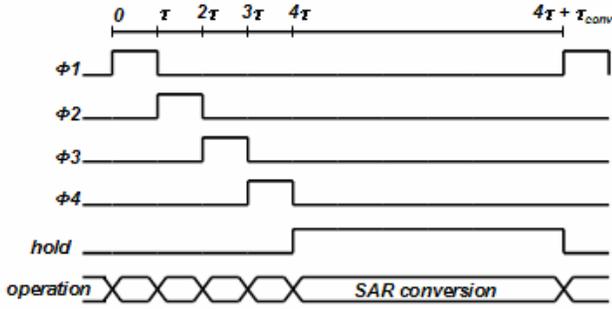


Fig. 3. Timing diagram of embedded FIR filter and SAR ADC operation.

II. EMBEDDED FIR FILTERING SCHEME

The charge sharing DT FIR filter is embedded in the sampling process of a SAR ADC. The SAR ADC capacitors are arranged into groups that are proportional to the relative coefficient sizes of an FIR filter. For example, the implementation of a 4-tap filter with coefficients [.25 .25 .25 .25] requires 4 groups of capacitors, as shown in Fig. 2. Assuming this particular arrangement, the input voltage is sampled onto capacitor group 1, 2, 3 and 4 at time 0, τ , 2τ and 3τ , respectively. The timing diagram for the filtering and SAR conversion process described above is shown in Fig. 3. After acquiring these four samples, all of the capacitor groups are charge shared, as shown in lower diagram of Fig. 2. This averages the previously sampled voltage levels and implements the FIR transfer function, $H(z)=(z^{-1}+z^{-2}+z^{-3}+z^{-4})/4$. The successive approximation operation that follows is identical to that of a SAR ADC without filtering, but produces filtered output code since it operates on a filtered input. Once the conversion process completes, the process described above repeats.

The timing diagram in Fig. 3 shows that multiple samples are collected during the sampling phase and no samples are collected during the conversion phase. Nonetheless, this non-uniform sampling results in the desired FIR filtering response. Exactly enough samples are collected during each sampling phase to generate a single filtered output sample, each of which is generated at the ADC conversion rate.

The overall ADC conversion rate, F_S , is described in (1), where n_{tap} is the number of taps of the selected filter and t_{conv} is the time required for A/D conversion.

$$F_S = 1/(n_{tap} \cdot \tau + t_{conv}) \quad (1)$$

The FIR filter is partly characterized by the input sampling rate, $F_{S,filter}$, which is the inverse of τ in (1). Since the ADC conversion rate, F_S , and the input sampling rate, $F_{S,filter}$ are not required to be the same, the embedded filter rate and response are highly reconfigurable.

As with any ADC, the conversion rate determines the Nyquist frequency, $F_S/2$, above which the input signal aliases. On the other hand, the input sampling rate determines the

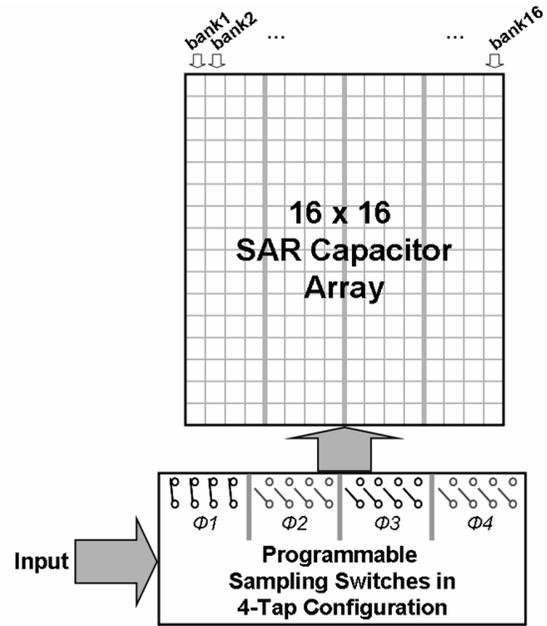


Fig. 4. High-level diagram of an embedded programmable filter in the DAC of a SAR ADC.

TABLE I
TESTED PROGRAMMABLE SAMPLING SWITCH CONFIGURATIONS

Filter Type	Filter Coefficient	-3dB frequency
No Filter	[16]/16	None
4-Tap	[4 4 4 4]/16	$2.0 \times F_S$
12-Tap #1	[1 1 1 2 1 2 2 1 2 1 1 1]/16	$1.4 \times F_S$
12-Tap #2	[4 0 1 1 1 1 1 1 1 1 0 4]/16	$1.0 \times F_S$

frequency span of the FIR filter response (i.e. $-\pi$ to π corresponds to $-F_{S,filter}/2$ to $F_{S,filter}/2$) and the frequency above which the filter response repeats. Inherent to the filter-ADC architecture, the input sampling rate is higher than the conversion rate, which allows the FIR filter to block multiple aliasing bands before the response repeats. The ideal and measured filter responses are discussed in section IV.

III. MODIFYING THE FILTER RESPONSE

The capacitive DAC in the prototype 9 bit SAR ADC contains 256 unit capacitors. These capacitors are grouped into 16 banks during the sampling phase, as shown in Fig 4. When the ADC operates without filtering, the analog input voltage is sampled onto all 16 capacitor banks simultaneously during the sampling period τ . When operating with the embedded FIR filter active, the 16 banks are arranged into multi-bank groups that are proportional to the relative coefficient sizes of an FIR filter with the desired frequency response.

The filter response can be modified by dividing the capacitor banks into different groupings and adjusting the sampling process appropriately. For example, a 12-tap filter with the coefficients [4 0 1 1 1 1 1 1 1 1 0 4]/16 can be realized by dividing the capacitor banks into 2 groups of 4 capacitor banks and 8 groups of 1 bank. Sampling occurs over 12 time periods (i.e. n_{tap} in (1) is 12). The fabricated prototype

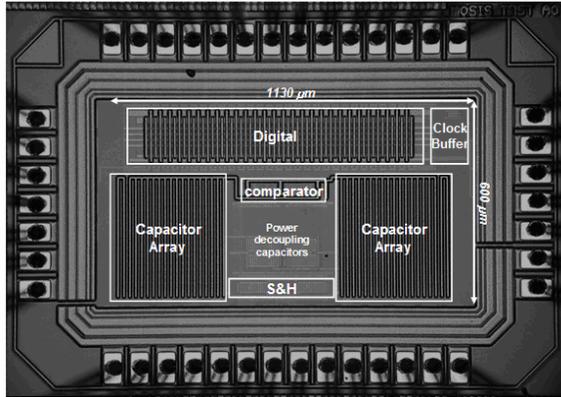


Fig. 5. Die microphotograph.

demonstrates the ability to customize the filter response by implementing 3 different arbitrarily chosen, externally controllable filtering responses. Table I summarizes the implemented filter configurations.

While three basic filtering modes are implemented to demonstrate the SAR ADC filtering technique, the architecture itself is highly adaptable to the dynamic filtering needs of a particular system. For example, the designer of a direct conversion receiver for a narrowband channel can divide the sampling capacitors into more banks, in order to enhance tap coefficient resolution. This permits precise placement of the filter nulls at multiples of F_S , thus allowing the filter to perform narrowband anti-aliasing. On the other hand, the designer of a receiver affected by unpredictable interferer frequencies and powers can program of the digital logic to support a variable number of tap coefficients, so that filter suppression can be enhanced or relaxed during system operation by increasing or decreasing the number of available filter zeros, respectively. Both of these changes require few modifications to the existing hardware. The first case typically requires only the addition of sampling related control lines and switches, since each capacitor bank of the DAC already consists of multiple unit-sized capacitors that can easily be regrouped. The second case typically requires little more than changing Verilog code.

IV. PROTOTYPE MEASUREMENTS

The reconfigurable FIR filter embedded in a SAR ADC is implemented in $0.13\mu\text{m}$ CMOS technology. The prototype occupies an active area of 0.68mm^2 including routing and power decoupling capacitors. Fig. 5 shows the die microphotograph of the prototype. The digital logic, including SAR logic and filter sampling control, is entirely synthesized from Verilog and auto-placed and routed. Simple changes to the Verilog code that implements SAR ADC control logic enable the filtering capability.

The measured attenuation at the lowest frequency notch is 30.5dB at $2.5 \times F_S$ for the 4-tap mode and 38.4dB at $1.7 \times F_S$ and 28dB at $1.1 \times F_S$ for the two 12-tap modes. Fig. 6 through Fig. 9 overlay the measured frequency response (in black) for all 4 modes of operation on top of the ideal FIR filter response (in grey).

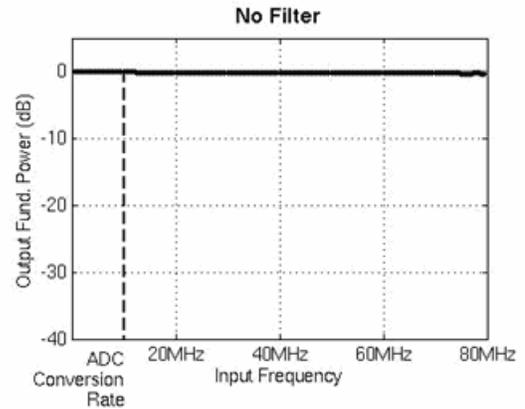


Fig. 6. Measured and ideal ADC response without filter turning on.

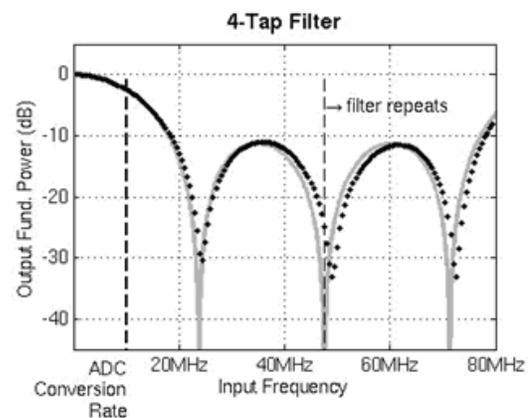


Fig. 7. Measured and ideal 4-tap [4 4 4 4]/16 filter response.

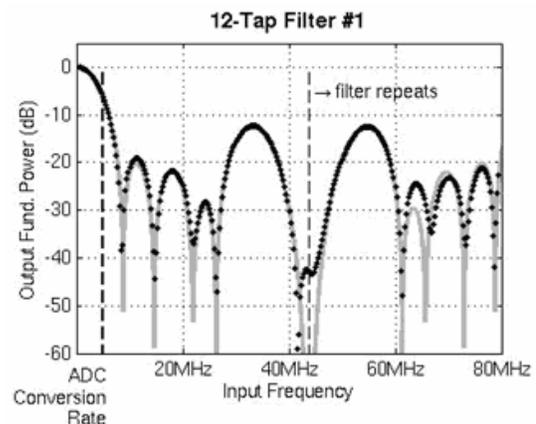


Fig. 8. Measured and ideal 12-tap [1 1 1 2 1 2 2 1 1 1]/16 filter response.

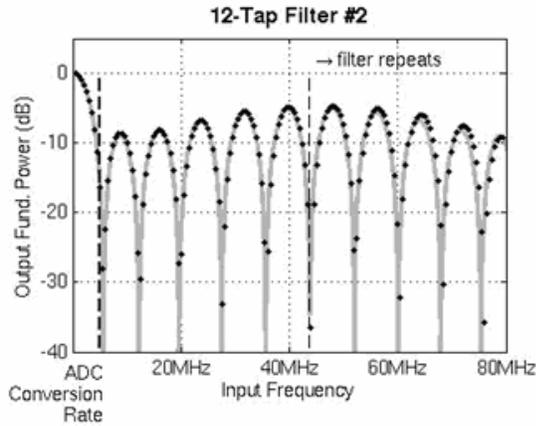


Fig. 9. Measured and ideal 12-tap [4 0 1 1 1 1 1 1 1 0 4]/16 filter response.

TABLE II
PERFORMANCE SUMMARY

Technology	1P8M 0.13 μ m CMOS with MIM capacitor			
Active Area	1.13 \times 0.60 mm ²			
Resolution	9b			
DNL/INL	< 0.9LSB / < 1.2LSB			
Filter Modes	No filter	4-tap filter	12-tap filter #1	12-tap filter #2
First notch attenuation and freq.	N/A	-30.5dB @ 2.5 \times F _s	-38.4dB @ 1.7 \times F _s	-28dB @ 1.1 \times F _s
ADC conversion rate	< 15MS/s	< 11MS/s	< 5.2MS/s	< 5.2MS/s
SNDR	48.9dB @ 12.5MS/s, 2MHz input	43.4dB @ 10MS/s, 0.5MHz input	45.0dB @ 5MS/s, 0.5MHz input	45.2dB @ 5MS/s, 0.5MHz input
Power @ 1MS/s	3.34mW	4.77mW	3.71mW	3.70mW
Power @ 5Ms/s	5.84mW	9.02mW	7.32mW	7.31mW

Table II summarizes the measured performance of the prototype. The ADC converts at up to 15MS/s without filtering enabled, 10MS/s with the 4-tap filter enabled and 5MS/s with the 12-tap filter enabled. Power consumption includes the power consumed by the internal clock buffer, digital, analog and excludes pad and external clock power.

Fig. 10 shows the measured output spectrum of a 2MHz input at 12.5MS/s conversion rate with no filtering. The measured SNDR and SFDR are 48.94dB and 54.36dB, respectively. Fig. 11 and Fig. 12 show DNL and INL plots of the 9b ADC. DNL and INL are within 0.9LSB and 1.2LSB, respectively.

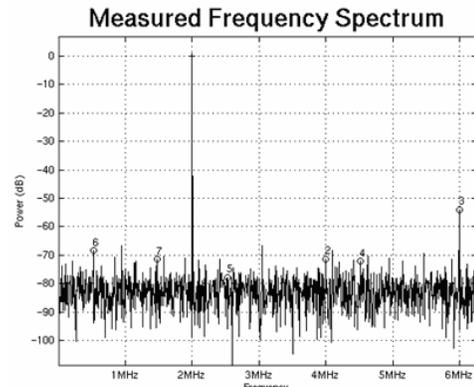


Fig. 10. Measured output spectrum at 12.5MS/s and 2MHz input.

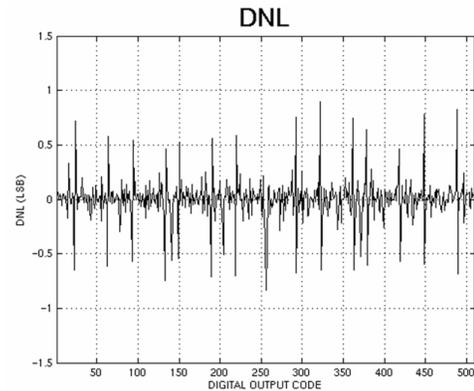


Fig. 11. Measured DNL plot.

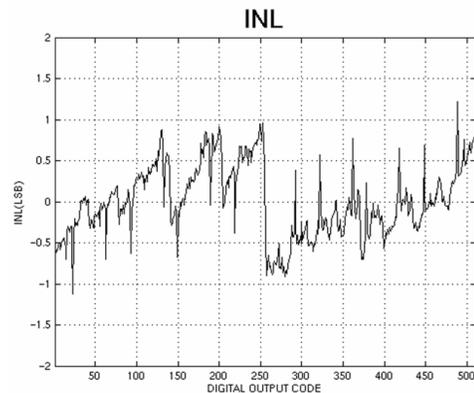


Fig. 12. Measured INL plot.

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