

# A 14b 23MS/s 48mW Resetting $\Sigma\Delta$ ADC with 87dB SFDR 11.7b ENOB & 0.5mm<sup>2</sup> area

Chun C. Lee and Michael P. Flynn

Department of EECS, University of Michigan, Ann Arbor, MI - 48109  
leechun@umich.edu

## Abstract

A 14b 23MS/s ADC that pipelines a 2<sup>nd</sup> order resetting  $\Sigma\Delta$  modulator with a 10b cyclic ADC and requires no front-end S/H is presented. The architecture uses a resetting  $\Sigma\Delta$  modulator at the front-end for accuracy and a cyclic ADC at the back-end for residual error quantization. This calibration-free ADC achieves no missing codes, 87dB SFDR and 11.7b ENOB. Fabricated in 0.18 $\mu$ m CMOS with a core area of 0.5mm<sup>2</sup>, it consumes 48mW from a 2V supply.

## Introduction

Many applications in communications, imaging and video demand high-resolution (>12b), low-distortion ADCs with a signal bandwidth of several MHz. Achieving this performance with Nyquist ADCs often requires calibration to enhance component matching and a front-end S/H [1]. CT  $\Sigma\Delta$  ADCs suffer from the requirement of RC time constant calibration and are sensitive to clock jitter. Low OSR (to achieve high-bandwidth) SC  $\Sigma\Delta$  ADCs, employing multi-bit feedback DAC, require calibration and/or dynamic element matching to maximize performance.  $\Sigma\Delta$  ADCs also require a digital decimation filter of considerable speed. Such additions increase power consumption, complexity and chip area.

This paper proposes a 2<sup>nd</sup> order resetting  $\Sigma\Delta$  modulator pipelined with a 10b cyclic ADC architecture. Such architectures have been used with high OSR, for low-frequency or DC input signal applications [2, 3]. This ADC uses a different  $\Sigma\Delta$  modulator loop from [2, 3], with a low OSR of 5 to eliminate the need of a front-end S/H and achieve higher bandwidth. Although it is calibration-free and has a low OSR, the prototype ADC achieves 11.7b ENOB, 87dB SFDR and no missing codes at 14b resolution. The resetting architecture eliminates the need for power hungry digital decimators and enables the ADC to sample as a Nyquist converter.

## Architecture

The proposed ADC architecture (Fig. 1) is a pipeline of a 2<sup>nd</sup> order resetting  $\Sigma\Delta$  modulator and a 10b cyclic ADC. The input is sampled and modulated at 115MHz, which is 5 times the conversion-rate, by the front-end  $\Sigma\Delta$  modulator. After every 5 samples, the residue ( $V_{res}$ ) at the output of the  $\Sigma\Delta$  front-end is passed to the cyclic ADC and the  $\Sigma\Delta$  modulator resets. The cyclic ADC then quantizes the residue while the  $\Sigma\Delta$  front-end processes the next 5 samples. The digital outputs from the  $\Sigma\Delta$  modulator and cyclic ADC are combined in the Digital Block to give overall output  $D_{out}$ . This 2-step pipelining leads to a latency of only 1 conversion-rate (23MS/s) clock period.

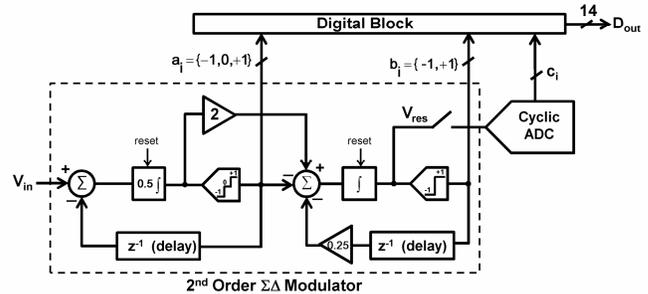


Fig. 1: ADC architecture

The 2<sup>nd</sup> order  $\Sigma\Delta$  front-end itself is a cascade of two 1<sup>st</sup> order modulators. The feed-back and feed-forward coefficients are chosen to maximize signal gain while avoiding clipping, and also to ensure large unit capacitors for more practical circuit implementation (Fig. 2). The output of the first integrator is 1.5b quantized (to  $a_i$ ) by 2 comparators with thresholds set at  $\pm V_{ref}/4$ . An inherently linear 1.5b DAC, driven by  $a_i$ , feeds the input of first integrator. The output of the second integrator is 1b quantized (to  $b_i$ ) by a single comparator with threshold set at 0.  $a_i$  and  $b_i$  together drive the input of the multi-bit DAC that feeds the second integrator. Assuming constant  $V_{in}$ , the output of the second integrator after 5 clocks is the residue ( $V_{res}$ ), which can be written as:

$$V_{res} = 15V_{in} - V_{ref} \left[ \sum_{i=1}^5 \sum_{j=1}^i a_j + \sum_{i=1}^4 (b_i / 4) \right] \quad (1)$$

The 10b cyclic ADC quantizes  $V_{res}$  giving a total ADC resolution of 13.9b.

For moving input signals,  $V_{in}$  in above equation is replaced by the linearly weighted average value, which causes low-pass-filtering with attenuation of up to 2.1dB at the 11.5MHz Nyquist frequency. This filtering can help anti-alias signals in some frequency ranges.

In this proposed modulator architecture, all comparators are fed only by SC integrators, and therefore see a sampled-and-held signal. This eliminates the need for a front-end S/H, unlike the case with the CIFF modulator used in [2, 3]. This is also an advantage over traditional pipeline ADC architectures which usually require front-end S/H to achieve low-distortion [1]. System-level simulations show that the architecture has a large tolerance towards circuit non-idealities. For example, 9b capacitor matching or 75dB op-amp gain is enough to ensure no missing codes at 14b resolution. This tolerance comes from a combination of choice of modulator architecture, modulator coefficients and the use of an inherently linear 1.5b DAC feeding the input of first integrator. A relaxed settling requirement helps in reducing op-amp power consumption. Oversampling in the front-end reduces thermal noise of the ADC. A full SC implementation ensures a high clock jitter tolerance of up to 3ps. All of the above lead to

a calibration-free, power-efficient and area-efficient design.

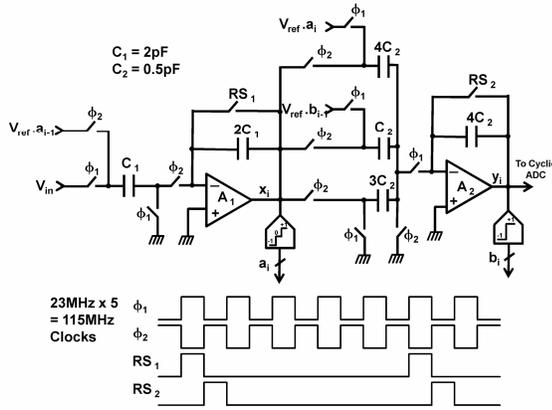


Fig. 2: SC implementation of 2nd order  $\Sigma\Delta$  modulator

### Circuit Implementation

#### A. Front-End $\Sigma\Delta$ Modulator

The SC implementation of the  $\Sigma\Delta$  front-end is shown in Fig. 2. Single-ended schematics are shown for clarity. The input sampling switches are bootstrapped for low distortion. Both op-amps are implemented as folded, single-stage, triple-cascode, NMOS-input having a gain of at least 75dB. Comparators have a relaxed offset requirement because of redundancy, and are implemented as preamplifiers followed by latches to reduce input referred offset and kickback.

#### B. 10b Cyclic ADC

The cyclic ADC is implemented using a single op-amp based on [4]. This ADC resolves 1.5b in each half clock period to yield 10b resolution in 5 clock cycles and consumes 8mW, or about 17% of the total power.

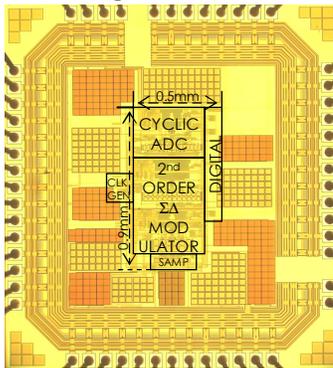


Fig. 3: Die micrograph

### Measurement Results and Conclusion

The prototype, fabricated in 1P6M 0.18 $\mu$ m CMOS, occupies a core area of 0.5mm<sup>2</sup>. It accepts a full scale input signal of 2V<sub>pp</sub> differential. The die micrograph is shown in Fig. 3. Fig. 4 shows the INL and DNL plots which indicate no missing codes at 14b level. A peak SNDR of 72dB (11.7b ENOB) is achieved for a 2MHz input. An 8192 point FFT plot, shown in Fig. 5, demonstrates 87dB SFDR for a 2MHz input signal at -0.5dB full scale. Fig. 6 summarizes the measured SFDR, SNDR for varying input frequencies. SFDR and SNDR fall to 81dB and 68dB respectively for a 10MHz input signal, this is partly due

to low-pass filtering discussed earlier. The chip consumes 48mW (analog: 40mW & digital: 8mW) at full conversion speed of 23MS/s.

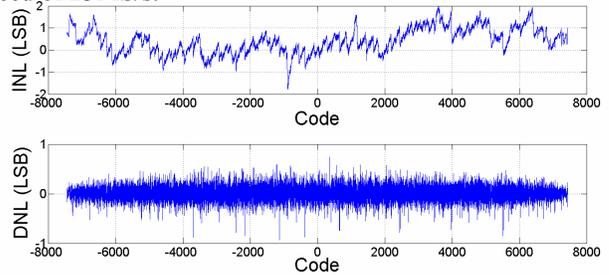


Fig. 4: Measured INL and DNL at 14b level

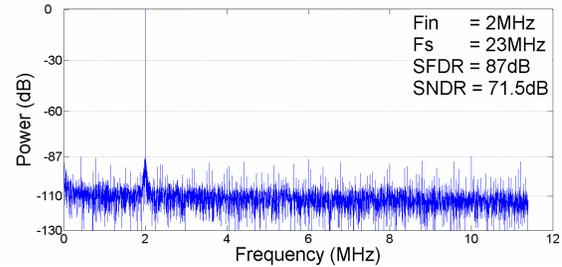


Fig. 5: 8192 point FFT plot for 2MHz input

This paper proposes a pipelined ADC architecture based on a resetting  $\Sigma\Delta$  modulator. Our experimental prototype demonstrates the ability of such an architecture to scale to high sampling speeds. In this prototype, a carefully designed front-end resetting  $\Sigma\Delta$  modulator pipelined with a simple cyclic ADC enhances the accuracy and speed of the ADC. This gives a calibration-free, power-efficient and area-efficient ADC design, which is often difficult to achieve in traditional ADC architectures.

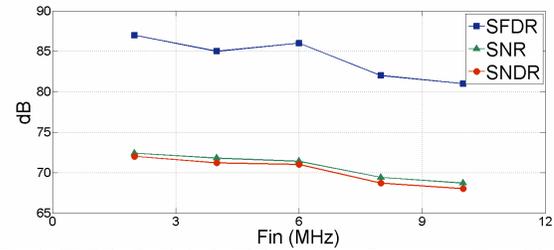


Fig 6: SFDR, SNR & SNDR vs. input frequency (Fs = 23MHz)

### Acknowledgements

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### References

- [1] D.Y. Chang, "Design Technique for a Pipelined ADC Without Using a Front-End Sample-and-Hold Amplifier," *IEEE Trans. Circuits Syst. I*, vol. 51, pp.2123-2132, Nov. 2004.
- [2] J. Markus, et al., "Theory and Applications of Incremental  $\Delta\Sigma$  Converters," *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 678-690, Apr. 2004.
- [3] A. Agah, et al., "A High-Resolution Low-Power Oversampling ADC with Extended-Range for Bio-Sensor Arrays," *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, pp. 244-245, June, 2007.
- [4] K. Nagaraj, "Efficient Circuit Configurations for Algorithmic Analog to Digital Converters," *IEEE Trans. Circuits Syst. II*, vol. 40, pp. 777-785, Dec. 1993.